Effects of ZrO_2/Al_2O_3 Gate-Stack on the Performance of Planar-Type InGaAs TFET

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***Abstract*— We investigate the impact of gate-stack engineering using $W/ZrO_2/Al_2O_3$ on the performance of planar-type InGaAs tunneling field-effect transistors (TFETs). It is shown that 1-nm-thick capacitance equivalent thickness (CET) with low leakage current is achieved by using ZrO_2 with the dielectric constant of around 40 on $In_{0.53}Ga_{0.47}As$. On the other hand, the reduction of D_{it} by insertion of ALD 1–5 cycle Al_2O_3 interfacial layers (ILs) is found to be mandatory for obtaining TFET performance enhancement. The planar-type InGaAs TFETs using the ZrO_2/Al_2O_3 IL gate-stack with CET of 1 nm exhibit the minimum subthreshold swing ($S.S_{min}$) of 55 mV/dec and I_{ON} of 0.88 $\mu A/\mu m$ (V_G–V_{OFF} = 0.5 V, V_D = 0.2 V, and I_{OFF} = 10 pA/μm). Furthermore, the ZrO_2/Al_2O_3 IL gate-stack is applied to the optimized $In_{0.75}Ga_{0.25}As$ quantum well (QW) channel TFETs. The low $S.S_{min}$ of 50 mV/dec and high I_{ON} of 1.2 $\mu A/\mu m$ (V_G–V_{OFF} = 0.5 V, V_D = 0.2 V, I_{OFF} = 10 pA/μm, and CET = 1.1 nm) are demonstrated by combing the present ZrO_2-based gate-stack with the optimum $In_{0.75}Ga_{0.25}As$ QW channel structure.**

***Index Terms*— InGaAs, ZrO_2, quantum well (QW), tunnel field-effect transistor (TFET).**

I. Introduction

TUNNEL field-effect transistor (TFET) is one of the most promising devices for ultralow power applications because of its steep subthreshold swing exceeding the MOSFET's thermal limits of 60 mV/dec at room temperature [1], [2]. For achieving high performance of TFETs, it is well known that a high gate controllability and abrupt tunneling junction with small and direct bandgap materials are generally important. Reported TFETs based on Si have suffered from the low on current (I_{ON}) and the sub-60 mV/dec subthreshold swing (S.S.) in an extremely low current level [3]–[5], suggesting that Si may not be an appropriate material for TFETs due to the low band-to-band (BTB) probability caused by the indirect and large bandgap. Thus, narrow and direct bandgap materials such as III–V compound semiconductors (InGaAs, InAs, and GaSb) are regarded as a possible solution of the TFET channel materials to achieve high I_{ON} and low sub-60mV/dec S.S. in a useful current range [5]–[16].

Recently, it has been demonstrated that a nanowire InAs/InGaAsSb/GaSb vertical TFET exhibits the minimum subthreshold swing ($S.S_{min}$) of 48 mV/dec and I_{ON} of 10 $\mu A/\mu m$ (V_{DD} = 0.3 V and I_{OFF} = 1 nA) [6]. A smaller effective bandgap obtained by using the type-II band structure such like InAs/GaSb as a tunneling junction can result in enhancement in the BTB tunneling efficiency [6]–[8]. However, this structure is not compatible with the standard complementary metal–oxide–semiconductor (CMOS) fabrication process.

On the other hand, the planar-type InGaAs TFETs with Zn diffused source, which are preferable in terms of compatibility with the CMOS process, have also realized the promising performance with $S.S_{min}$ of 64 mV/dec and I_{ON} higher than 1 $\mu A/\mu m$ at low drain voltage (V_D) of 0.15 V_D[11]. Here, the Zn diffusion into InGaAs from spin-on-glass (SOG), allowing to automatically realize a steep Zn profile with less defect generation, is employed to form the abrupt tunneling junction with reduced leakage currents. Moreover, TFETs using the high-In-content $In_xGa_{1-x}As$, which boosts up the BTB tunneling current, have obtained the higher I_{ON} with increased I_{OFF} due to the reduced bandgap [11], [12]. In order to simultaneously realize the enhancement of the BTB tunneling current and suppression of the increase in I_{OFF}, the quantum well (QW) structure of $In_{0.53}Ga_{0.47}As$/high-In-content $In_xGa_{1-x}As/In_{0.53}Ga_{0.47}As$ has been proposed for an channel of planar-type InGaAs TFETs [13], [14]. The InGaAs QW TFET with 3-nm-thick $In_{0.67}Ga_{0.33}As$ have achieved the $S.S_{min}$ of 54 mV/dec at capacitance equivalent thickness (CET) of 1.4 nm [15]. However, further improvements are still required to increase the current level in the V_g region, where S.S. is lower than 60 mV/dec in order to surpass the performance of CMOS under ultralow voltage operation.

Here, the increase in gate controllability by using gate-stacks with thinner equivalent oxide thickness (EOT) is an important direction to improve the TFET performance. Actually, the $In_{0.53}Ga_{0.47}As$ TFETs using HfO_2/Al_2O_3gate-stacks with CET of 1.4 and 1.3 nm have achieved $S.S_{min}$ of 57 and 54 mV/dec, respectively [15], [16]. In this paper,

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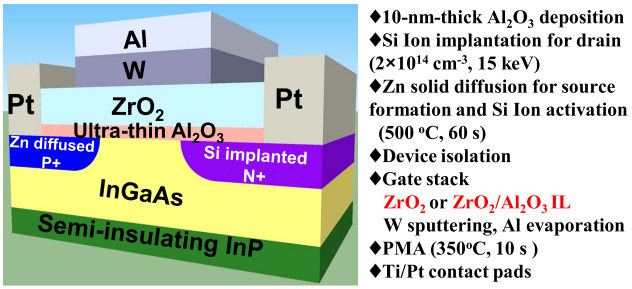

Fig. 1. Schematic structure and the fabrication process of an InGaAs TFET with a Zn diffused source.

EOT scaling of planar-type InGaAs TFET with maintaining superior MOS interface properties is further pursued by using ZrO_2 as one of the higher dielectric constant (k) gate insulators [17]–[20]. We also investigate the ZrO_2/InGaAs MOS interface properties and demonstrate the effectiveness of insertion of ultrathin Al_2O_3 between ZrO_2 and InGaAs on reduction in both interface state density (D_{it}) and CET. The impact of gate-stacks using ZrO_2 and Al_2O_3 interfacial layers (ILs) on the performance of planar-type InGaAs TFETs is examined quantitatively. Besides, steepness of Zn profiles in $In_xGa_{1-x}As$ with different In contents (x) is evaluated to optimize the In content of $In_xGa_{1-x}As$ QW. The optimized $In_xGa_{1-x}As$ QW and gate-stack using ZrO_2 and Al_2O_3 ILs are combined to achieve the high performance.

II. Device Fabrication

A. $In_{0.53}Ga_{0.47}As$ MOS Capacitor

n-$In_{0.53}Ga_{0.47}As$ with an Si impurity concentration of 5×10^{15} cm^{-3} grown on an InP (001) substrate by metal organic vapor phase epitaxy (MOVPE) is used to fabricate an InGaAs MOS capacitor. After pretreatment using acetone for 1 min, a 29% NH_3 solution for 1 min and a $(NH_4)_2S_x$ solution with 0.6%–1% S concentration for 5 min, ZrO_2 films are deposited on InGaAs by ALD (atomic layer deposition) using $Zr[NCH_3C_2H_5]_4$ and H_2O as precursors. The (1–5)-cycle Al_2O_3 ILs are introduced in order to modify the MOS interface properties. The 20-nm-thick W is sputtered as a gate metal, followed by evaporation of 100-nm-thick Al as a top contact pad. For a back contact pad, Al is deposited by thermal evaporation. Postmetal annealing (PMA) is performed at 350 °C for 10 s.

B. Planar-Type InGaAs TFET With Zn Diffused Source

Fig. 1 shows the schematic structure and the fabrication flow of a planar-type InGaAs TFET with a Zn diffused source. A 100-nm-thick $In_{0.53}Ga_{0.47}As$ layer is grown on a semiinsulating InP (001) substrate by MOVPE. As a diffusion mask for selective Zn diffusion and a sacrificial layer for suppressing implantation damages, a 10-nm-thick Al_2O_3 film is deposited by ALD at 200 °C. Si ions implantation into the drain region is carried out with a dose of 2×10^{14} cm^{-3} and an acceleration energy of 15 keV. After etching Al_2O_3 on the source region, a Zn SOG film is coated by using a spin coater at 3750 r/min. The Zn SOG film is cured using

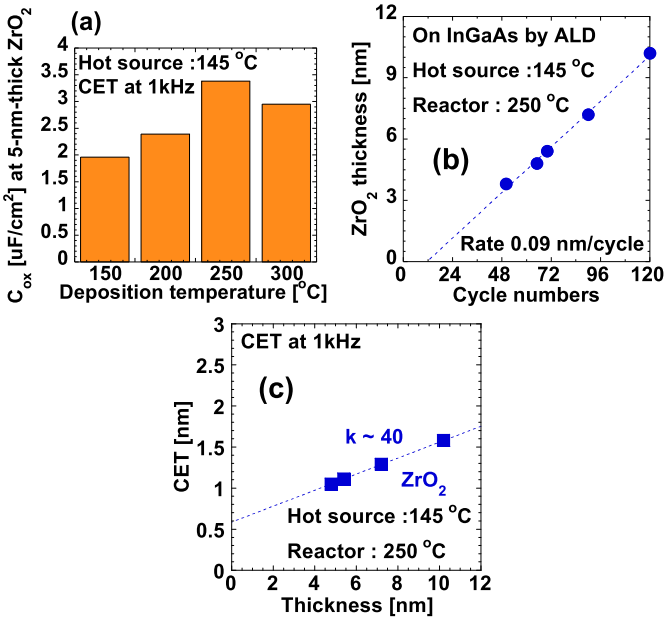

Fig. 2. (a) Deposition temperature dependence of ZrO_2 on $In_{0.53}Ga_{0.47}As$ and (b) ZrO_2 thickness as a function of the ALD cycle number on InGaAs at 250 °C and (c) dielectric constant (k◁ of ZrO_2 on InGaAs at 250 °C.

a hot plate at 200 °C for 2 h. The selective Zn diffusion is driven by rapid thermal annealing at 500 °C for 1 min in N_2 gas ambient. The unreacted SOG film and the Al_2O_3 diffusion mask are removed by a diluted HF solution. In order to flatten the InGaAs surface after Zn diffusion, the sample is dipped into N.N-dimethylformamide at 150 °C for 2 h, followed by buffered HF cleaning for 10 min. Each device is isolated by selectively etching InGaAs with a mixture solution of H_3PO_4, H_2O_2, and H_2O. The pretreatment using acetone for 1 min, a 29% NH_3 solution for 1 min and a $(NH_4)_2S_x$ solution with 0.6%–1% S concentration for 5 min is carried out to remove a native oxide and to passivate the surface with sulfur (S) atoms. The 1.9-nm-thick ZrO_2/(1, 2, and 3)-cycle Al_2O_3 films and 2.1-nm-thick ZrO_2/5-cycle Al_2O_3 with CET of 1.03, 1.0, 1.09, 1.17, and 1.56 nm, respectively, estimated from the InGaAs MOS capacitors, are deposited on InGaAs by ALD. The Al/W gate metal formation and PMA are the same as in the MOS capacitor fabrication. Finally, Ti/Pt is sputtered for the source/drain contact pads, after etching ZrO_2/Al_2O_3 layers on the source/drain regions by a diluted HF solution.

III. Device Characteristics and Discussion

Improvement in crystallinity of ZrO_2 is important for obtaining the high k value of ZrO_2. One of the most important factors for crystallinity of ALD ZrO_2 is the deposition temperature. Thus, the deposition temperature dependence of ZrO_2 on InGaAs is examined by using 5-nm-thick ZrO_2/InGaAs MOS capacitors with changing the deposition temperature from 150 °C to 300 °C. Fig. 2(a) shows C_{max} at $V_G = 1.5$ V of the 5-nm- thick ZrO_2/InGaAs MOS capacitors as a function of deposition temperature. It is found that C_{max} of the InGaAs MOS capacitor with ZrO_2 deposited at 250 °C is highest, meaning the highest permittivity of ZrO_2. Fig. 2(b)

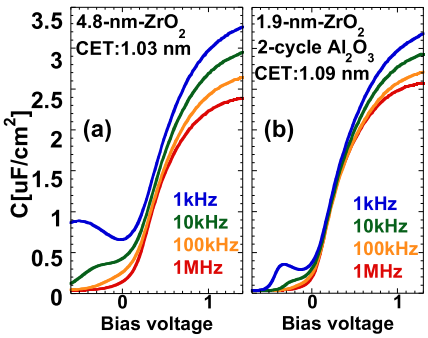

Fig. 3. *C–V* curves of $In_{0.53}Ga_{0.47}As$ MOSCAP with (a) 60-cycle-ZrO_2(4.8 nm) and (b) 35-cycle-ZrO_2 (1.9 nm)/2-cycle-Al_2O_3 IL.

shows the ZrO_2 thickness as a function of the ALD cycle number on InGaAs at 250 °C, indicating the deposition rate of 0.09 nm/cycle and the incubation time of around 12 cycles. The k value of around 40 is obtained for ZrO_2 on InGaAs at ALD temperature of 250 °C, as shown in Fig. 2(c). This k value of ZrO_2 on InGaAs is slightly high in comparison with the previously reported k values of 30 ± 1 [17] and 32 [18], attributable to optimized ALD deposition temperature. Also, it has been reported for the Si MOS capacitors that the ZrO_2k value of 35±2 [19] and 53 [20] can be achieved by improving the crystallinity of ZrO_2 film.

Fig. 3(a) shows the C–V curves of an Al/W/60-cycle-ZrO_2(4.8 nm)/InGaAs MOS capacitor. The CET value of 1.03 nm is achieved at 1 MHz with the low gate leakage current of 6×10^{-7} A/cm^{-2} at $V_G = V_{fb} + 1$ V. However, the ZrO_2/InGaAs direct interface exhibits the high-frequency dispersion in the accumulation region and large hump in the inversion region, suggesting the high interface trap density (D_{it}). The energy distributions of D_{it} for the ZrO_2/InGaAs MOS capacitor without Al_2O_3, evaluated by the conductance method, are shown in Fig. 4(a). The D_{it} of ZrO_2/InGaAs is higher than $\sim 10^{13}$ eV^{-1}cm^{-2}, which is similar to the reported values [17], [18].

It is well known for HfO_2 gate-stack on InGaAs that the insertion of Al_2O_3 ILs between HfO_2 and InGaAs is effective for reduction in D_{it}, because the Al_2O_3/InGaAs interface exhibits low D_{it} of $\sim 10^{12}$ eV^{-1}cm^{-2} [21]–[24]. Thus, Al_2O_3 ILs only with a few cycle are introduced between ZrO_2 and InGaAs to reduce D_{it} with minimizing an increase in CET. Fig. 3(b) shows the C–V curves of an Al/W/35-cycle-ZrO_2 (1.9 nm)/2-cycle-Al_2O_3/InGaAs MOS capacitor. Here, both the frequency dispersion in accumulation region and the hump in the inversion region are suppressed by inserting the Al_2O_3 IL, in comparison with the ZrO_2/InGaAs direct interface. It is found in Fig. 4(a) that (1 to 5)-cycle-Al_2O_3 ILs can significantly decrease D_{it} at the ZrO_2/InGaAs interface. The minimum D_{it} of 5×10^{12} eV^{-1}cm^{-2} and 3×10^{12} eV^{-1}cm^{-2} are obtained for the InGaAs MOS capacitors with ZrO_2/1-cycle Al_2O_3 and ZrO_2/2-to-5-cycle Al_2O_3 ILs, respectively. On the other hand, CET of the ZrO_2/ Al_2O_3 ILs/InGaAs MOS capacitors also rapidly increase because of the low-k Al_2O_3 layer in spite of the ultrathin thickness, as shown in Fig. 4(b). As a result, we can conclude that the two-cycle-Al_2O_3 is the optimal IL thickness for the ZrO_2/ InGaAs MOS interface in

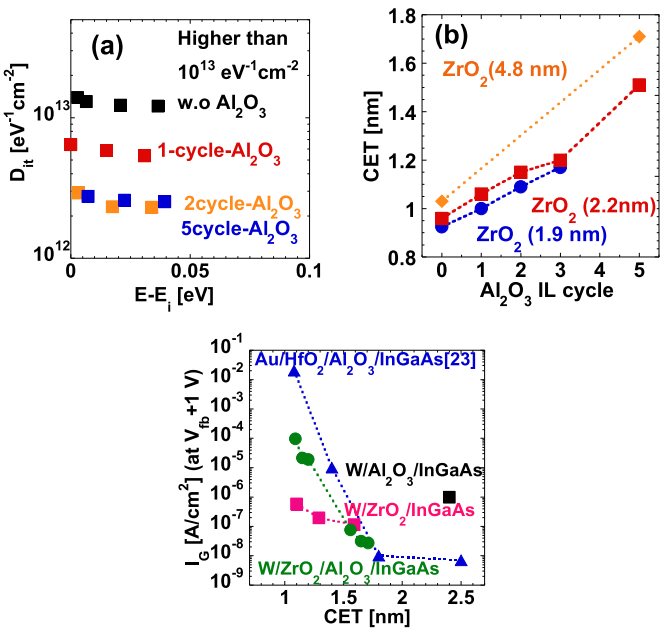

Fig. 4. (a) D_{it} distributions of $In_{0.53}Ga_{0.47}As$ MOSCAP with ZrO_2/(0-to-5-cycle) Al_2O_3IL. (b) CET versus Al_2O_3 IL cycle of $In_{0.53}Ga_{0.47}As$ MOSCAPs with ZrO_2/Al_2O_3. (c) Comparison in the gate leakage current as a function of CET among Al_2O_3 (black), HfO_2/Al_2O_3(bule), ZrO_2(pink), and ZrO_2/Al_2O_3 (green) on InGaAs.

order to achieve low D_{it} with minimizing an increase in CET. The gate leakage current of ZrO_2/InGaAs MOS capacitor is also examined. Fig. 4(c) shows the gate leakage current of ZrO_2, HfO_2, and Al_2O_3 on InGaAs as a function of CET. It is found that ZrO_2/Al_2O_3/InGaAs exhibits lower gate current in a thin CET region than HfO_2/Al_2O_3/ InGaAs, attributed mainly to the higher k value (relative permittivity) of ZrO_2 than that of HfO_2. Under the same CET value, ZrO_2 thickness can be thicker than that of HfO_2, leading to the reduction in direct tunneling current. In addition, Goel *et al.* [17] have also pointed out that the conduction band offset between ZrO_2 and InGaAs can be higher than that between HfO_2 and InGaAs. This increase in the band offset for ZrO_2 can also decrease the direct tunneling current in comparison with HfO_2 under the same physical thickness.

Fig. 5(a) shows the source current (I_S)–(V_G–V_{OFF}) characteristics of a Zn diffused InGaAs TFET with the ZrO_2/Al_2O_3 gate-stack. The channel length (L_{ch}) and width (W) of TFETs is 15 and 90 μm, respectively. Here, V_{OFF} is the off voltage, defined as gate voltage at I_S of 10 pA/μm. Note that I_S is identical to I_D and gate leakage current (I_G) is lower than I_S, as shown in Fig. 5(a). The transfer characteristics of the InGaAs TFETs with the ZrO_2 gate-stack are greatly improved by inserting the Al_2O_3 ILs. The Zn-diffused-source InGaAs TFETs with ZrO_2/Al_2O_3 ILs at CET of 1, 1.09, 1.17, and 1.56 nm exhibit I_{ON} of 0.88, 0.83, 0.64, and 0.68 μA/μm (V_G–V_{OFF} = 0.5 V, V_D = 0.2 V, and I_{OFF} = 10 pA/μm), which is higher than I_{ON} of 0.026 μA/μm in the InGaAs TFET without Al_2O_3 ILs, whose CET is 1.03 nm. Also, the insertion of Al_2O_3 ILs between ZrO_2 and InGaAs improves the I_{ON}/I_{OFF} ratio from $\sim 10^4$ to $\sim 10^6$, attributed to reduction in D_{it}. The hysteresis characteristics of the InGaAs TFET with ZrO_2

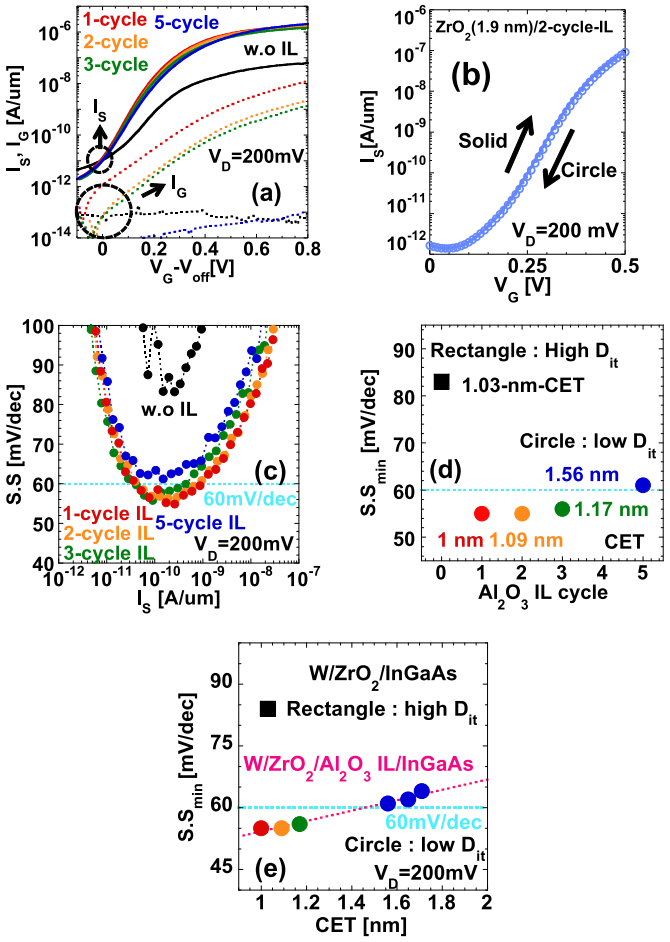

Fig. 5. (a) I_S-(V_G–V_{OFF}) characteristics and (b) hysteresis characteristics with double V_G sweep from 0 to 0.5 V. (c) S.S-I_S characteristics and (d) $S.S_{min}$-deposition cycle number of Al_2O_3 IL relationship. (e) $S.S_{min}$-CET relationship of $In_{0.53}Ga_{0.47}As$ TFET with 1.9-nm-ZrO_2/(0–5)- cycle-Al_2O_3 IL(V_{OFF} = 0 V at I_S = 10 pA/μm).

(1.9 nm)/Al_2O_3 (two cycle) are examined by sweeping V_G between 0 and 0.5 V in forward and backward ways. The result is shown in Fig. 5(b). The amount of hysteresis at I_S of 10^{-9} A/μm is as small as 3 mV.

Fig. 5(c) shows the S.S.-I_S characteristics of the InGaAs TFET with ZrO_2/Al_2O_3 ILs. Here, I_S is used to extract S.S. The minimum subthreshold swing ($S.S_{min}$) of 55–57mV/dec are achieved for the InGaAs TFET using ZrO_2/Al_2O_3 ILs with (1–1.17)-nm-thick CET, while the 1.03-nm-thick CET InGaAs TFET without Al_2O_3 ILs exhibits $S.S_{min}$ of 84 mV/dec. Fig. 5(d) shows $S.S_{min}$ as a function of IL Al_2O_3 cycle. It is found that the (1–5)-cycle Al_2O_3 ILs are sufficient to improve the S.S. of the planar-type InGaAs TFETs with the Zn-diffused sources. The reduction in D_{it} in the InGaAs channel region can improve the sensitivity of the surface potential modulation in the channel region to V_G. Therefore, we can conclude that not only thin CET but also low D_{it} is strongly required for achieving steep S.S. characteristics and high I_{ON} of TFETs. Fig. 5(e) shows the relationship between $S.S_{min}$ and CET of the $In_{0.53}Ga_{0.47}As$ TFET with 1.9-nm-ZrO_2/(0–5)-cycle-Al_2O_3 ILs. It is found that S.S. of the InGaAs TFETs monotonically decreases with a decrease in CET under sufficiently low D_{it}.

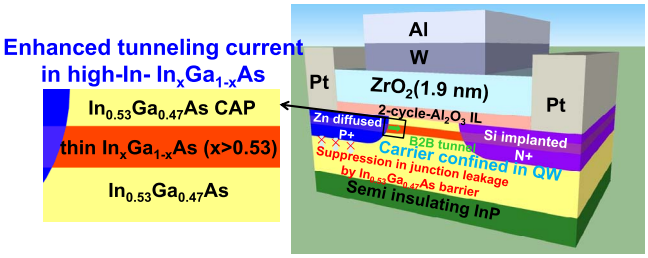

Fig. 6. Schematic of $In_xGa_{1-x}As$ QW TFET with 35-cycle-ZrO_2/2-cycle-Al_2O_3 gate-stack. High-In-content InGaAs enhances the BTB tunneling current.

In order to further improve the performance of planar-type InGaAs TFETs, the gate-stack of W/ZrO_2 (1.9 nm)/Al_2O_3 (two cycle), which satisfies thin CET and low D_{it} simultaneously, is applied to $In_{0.53}Ga_{0.47}As$/high-In-content $In_xGa_{1-x}As$ (x > 0.53)/$In_{0.53}Ga_{0.47}As$ QW ($In_xGa_{1-x}As$ QW) TFETs. Fig. 6 shows the schematic structure. This structure allows us to enhance the BTB tunneling current of planar-type TFETs by the smaller bandgap of high-In-content $In_xGa_{1-x}As$ in QW located near the MOS interface and to suppress the junction leakage current induced by Shockley–Read–Hall generation/ recombination process thanks to the barrier layer of low-In-content $In_{0.53}Ga_{0.47}As$ [14].

Meanwhile, the steep Zn profile in InGaAs realized by Zn diffusion from SOG is a key for the superior performance of planar-type InGaAs TFETs [11]. While the steepness of the Zn profiles has been confirmed for $In_{0.53}Ga_{0.47}As$ [11], the In content dependence has not been studied yet. Thus, the Zn profile in $In_xGa_{1-x}As$ with different In contents (x) is evaluated by using a secondary ion mass spectrometry (SIMS) analysis. Here, $In_xGa_{1-x}As$ with the In contents of 0.53, 0.6, 0.7, 0.8, and 0.9 on InP, and bulk InAs are used. Since the surface morphology of InAs grown on InP was quite poor, bulk InAs is used for the present experiments. In order to avoid the underestimation in steepness of the Zn profiles in InGaAs attributed to the atom mixing effect during the SIMS analysis, the Zn profile in InGaAs is analyzed at an extremely low energy of 0.5 keV using Cs^+ ions. But this SIMS analysis with low Cs^+ ions energy limits the measurable depth to around 100 nm. Therefore, it should be noted that Zn diffusion from SOG is performed at 450 °C for 60 s in $In_xGa_{1-x}As$ with different x to form sufficiently thinner Zn diffusion depth than 100 nm for the accurate SIMS analysis in this experiment, while Zn is diffused at 500 °C for TFET fabrication. Fig. 7(a) shows the Zn diffusion profiles in $In_xGa_{1-x}As$ with different x. It is shown that the Zn diffusion depth becomes thicker with higher x. In x > 0.8, the Zn doping concentration decreases with an increase in x. Here, the steepness of the Zn profile is defined in a Zn concentration range from 1×10^{18} cm^{-3} to 9×10^{18} cm^{-3}. Fig. 7(b) shows the steepness of the Zn profile as a function of x. The steepness of the Zn profile in $In_xGa_{1-x}As$ with x of 0.53–0.7 exhibits around 4 nm/dec, which is similar to the reported values [11], [13]. However, the steepness of the Zn profile starts to be degraded from the In content of 0.8.

The mechanism of Zn diffusion in InGaAs is well explained by the interstitial–substitutional model [25]–[28]. According

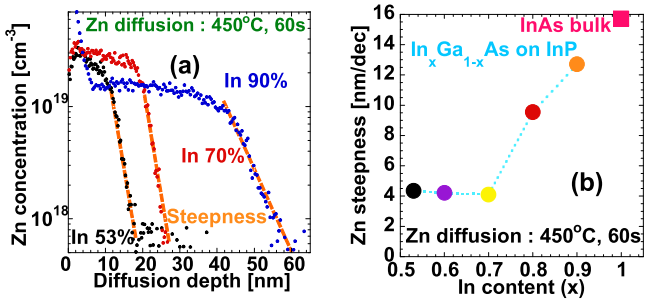

Fig. 7. (a) Zn profiles and (b) Zn concentration steepness in $In_xGa_{1-x}As$ with different In contents (x).

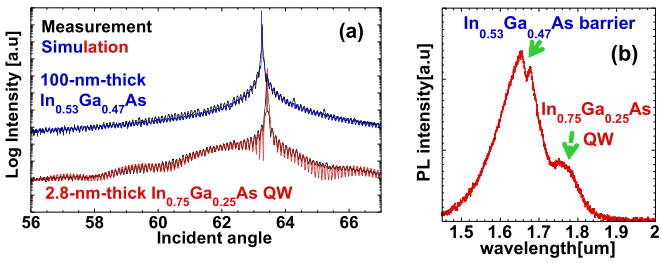

Fig. 8. (a) XRD spectra of 100-nm-thick $In_{0.53}Ga_{0.47}As$ (blue) and 2.8-nm-thick $In_{0.75}Ga_{0.25}As$ QW (red) and (b) PL spectra of 2.8-nm-thick $In_{0.75}Ga_{0.25}As$ QW. Estimated bandgap by is 0.7 eV.

to this model, the Zn diffusion coefficient in $In_xGa_{1-x}As$ is proportional to the concentration of singly ionized Zn^+ ion or the square of doubly-ionized Zn^{2+} ion concentration under the extrinsic conditions ([Zn] $\gg$ n_i) [26]. In general, the doping profile becomes steeper when the diffusion coefficient is proportional to the term with the higher-order dependence of doping concentration [11]. It has been reported that the Zn diffusion coefficient in GaAs and $In_{0.53}Ga_{0.47}As$ is proportional to the square of Zn concentration [25]–[28], while that in InAs is proportional to the Zn concentration [28]. As a result, the Zn profile in $In_{0.53}Ga_{0.47}As$ is steeper than that in InAs. These previous results are consistent with the present experimental finding that an increase in the In content causes degradation in steepness of the Zn profile in InGaAs, shown in Fig. 8(a) and (b).

Based on the present experiments of the In content dependence of the steepness, $In_xGa_{1-x}As$ with the In content of around 0.7 is used as a QW layer to avoid the degradation in steepness of the Zn profile. The thickness of QW is designed with 3 nm to suppress the defects generation [14]. An $In_{0.53}Ga_{0.47}As$/high-In-content $In_xGa_{1-x}As$ ($x > 0.53$)/$In_{0.53}Ga_{0.47}As$ QW is grown by MOVPE. X-ray diffraction (XRD) is used for evaluating the In content and well thickness of $In_xGa_{1-x}As$ QW. The XRD result indicates that the In content (x) and the well thickness of $In_xGa_{1-x}As$ QW is 0.75 and 2.8 nm, respectively, as shown in Fig. 8(a). The effective bandgap of 2.8-nm-thick $In_{0.75}Ga_{0.25}As$ estimated by the photoluminescence spectra at a low exciting laser power is estimated to be 0.7 eV, as shown in Fig. 8(b).

Fig. 9(a)–(c) shows the transfer characteristics, the I_S-S.S. characteristics and the I_S–V_D characteristics of a 2.8-nm-thick $In_{0.75}Ga_{0.25}As$ QW TFET with the gate-stack of the W/1.9-nm ZrO_2/2-cycle Al_2O_3 IL. The channel length

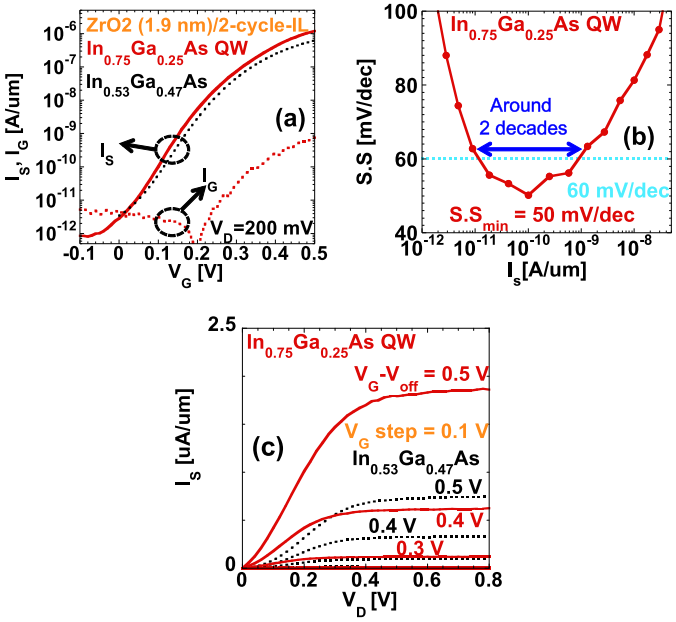

Fig. 9. (a) Transfer characteristics of the $In_{0.75}Ga_{0.25}As$ QW TFET with 35-cycle-ZrO_2/2-cycle-Al_2O_3. (b) S.S-I_S characteristics of $In_{0.75}Ga_{0.25}As$ QW TFET with 35-cycle-ZrO_2/2-cycle-Al_2O_3. (c) I_S–V_D characteristics of $In_{0.75}Ga_{0.25}As$ QW TFET and $In_{0.53}Ga_{0.47}As$ TFET (V_{OFF} at I_S = 10 pA/μm).

TABLE I
BENCHMARK OF CET, S.S$_{min}$, I_{ON}, AND I_{SUB-60} RANGE FOR PLANAR-TYPE InGaAs TFET

Channel Material (Gate stack)	CET [nm]	S.S$_{min}$ [mV/dec]	I_{on}[A/um] (V_G-V_{off}=0.5, V_D=0.2 V, I_{off} = 10 pA/um)	I_{sub-60} range [A/um] V_D=0.2 V
$In_{0.53}Ga_{0.47}As$[11] (Al_2O_3)	1.4 (EOT)	64	~ 6×10^{-7}	N/A
$In_{0.7}Ga_{0.3}A$[12] (Al_2O_3/HfO_2)	1.5	60	~ 6×10^{-7}	N/A
$In_{0.67}Ga_{0.33}As$[14] (Al_2O_3)	2.4	62	4.8×10^{-7} (V_D=0.15V)	N/A
$In_{0.53}Ga_{0.47}As$[15] (Al_2O_3/HfO_2)	1.3	54	~ 8×10^{-7}	2.5×10^{-11}~7.5×10^{-10}
$In_{0.67}Ga_{0.33}As$[16] (Al_2O_3/HfO_2)	1.4	54	7×10^{-7}	1.9×10^{-11}~6.7×10^{-10}
$In_{0.53}Ga_{0.47}As$ (Al_2O_3/ZrO_2)	1	55	8.8×10^{-7}	4×10^{-11}~9.5×10^{-10}
$In_{0.75}Ga_{0.25}As$ (Al_2O_3/ZrO_2) This work	1.1	50	1.2×10^{-6}	1.3×10^{-11}~1.1×10^{-9}

(L_{ch}) and width (W) of the QW is 40 and 90 μm, respectively. The $In_{0.75}Ga_{0.25}As$ QW TFET shows the improved transfer characteristics by the enhanced tunneling efficiency in the $In_{0.75}Ga_{0.25}As$ QW layer, in comparison with the $In_{0.53}Ga_{0.47}As$ bulk TFET. Here, S.S$_{min}$ of 50 mV/dec and sub-60 mV/dec S.S. over around two decades of I_S are achieved by combing the optimized ZrO_2/Al_2O_3 gate-stack (1.1-nm-thick CET and low D_{it} of $\sim 3 \times 10^{12}eV^{-1}cm^{-2}$) with the 2.8-nm-thick $In_{0.75}Ga_{0.25}As$ QW structure. Also, the present $In_{0.75}Ga_{0.25}As$ QW TFET provides higher I_{ON} of 1.2 μA/μm at V_G–V_{th} = 0.5 V, V_D = 0.2 V, and I_{OFF} = 10 pA/μm than that of the $In_{0.53}Ga_{0.47}As$ bulk TFET, as shown in Fig. 9(a) and (c).

Table I shows the benchmark of CET, S.S$_{min}$, I_{ON}, I_{sub-60} range which is defined as the current range with S.S. less than 60 mV/dec among the reported planar-type InGaAs

TFETs [11]–[16]. Thin CET is effective in reducing $S.S_{min}$ of the InGaAs TFETs. It is found that $S.S_{min}$ of 50mV/dec for the present 2.8-nm-thick $In_{0.75}Ga_{0.25}As$ QW TFET is the record-low value among the reported InGaAs TFETs, thanks to the combination of the gate-stack engineering using ZrO_2 and the high-In-content $In_xGa_{1-x}As$ QW.

IV. Conclusion

We have improved the performance of planar-type InGaAs TFETs by using gate-stack engineering using ZrO_2/Al_2O_3 ILs. The planar-type InGaAs TFETs with CET of 1–1.2 nm and D_{it} of around 3–5 $\times$ 10^{12} $eV^{-1}cm^{-2}$ exhibit $S.S_{min}$ of 55–57 mV/dec at $V_D = 0.2$ V. Furthermore, the 2.8-nm-thick $In_{0.75}Ga_{0.25}As$ QW TFET with CET of 1.1-nm have yielded $S.S_{min}$ of 50 mV/dec at $V_D = 0.2$ V and I_{ON} of 1.2 $\mu A/\mu m$ at $V_G - V_{th} = 0.5$ V, $V_D = 0.2$ V, and $I_{OFF} = 10$ pA/μm.

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