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Design and properties of planar-type tunnel FETs using $In_{0.53}Ga_{0.47}As/In_xGa_{1-x}As/In_{0.53}Ga_{0.47}As$ quantum well

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Tunnel Field Effect Transistors (tunnel FETs) have been proposed using $In_{0.53}Ga_{0.47}As/In_xGa_{1-x}As/In_{0.53}Ga_{0.47}As$ Quantum Well ($In_xGa_{1-x}As$ QW) channels which improve their performance. It is expected in this structure that the high-In-content $In_xGa_{1-x}As$ QW layer with the lower bandgap can increase the tunneling current and resulting on-current (I_{on}), while the low-In-content $In_{0.53}Ga_{0.47}As$ layer, where the source junction edge is mainly formed, can suppress the increase in the junction leakage current because of the higher bandgap. Considering the strain effect and the quantum confinement effect of the $In_xGa_{1-x}As$ QW layers, the In content and the QW thickness are designed carefully in terms of the reduction in the effective bandgap. The proposed tunnel FETs using the QW layers grown by Metal-organic Vapor Phase Epitaxy are fabricated, and the electrical and physical properties are systematically evaluated. It is found that the $In_xGa_{1-x}As$ QW can significantly enhance the performance of tunnel FETs. As expected in the calculation of the effective bandgap, the higher In content and thicker QW thickness lead to higher I_{on}, while the thinner QW thickness makes the sub-threshold swing (S.S.) steeper through the reduction in off-current (I_{off}) and enhancement of carrier confinement. The minimum sub-threshold swing ($S.S._{min}$) of 62 mV/dec is obtained at $V_D = 150$ mV for a tunnel FET with an $In_{0.53}Ga_{0.47}As$ (2.6 nm)/$In_{0.67}Ga_{0.33}As$ (3.2 nm)/$In_{0.53}Ga_{0.47}As$ (96.3 nm) QW structure. Also, the highest I_{on} of 11 $\mu A/\mu m$ at $V_D = 150$ mV and $V_G = 1$ V, which is 8.5 times higher than 1.3 $\mu A/\mu m$ of a control $In_{0.53}Ga_{0.47}As$ tunnel FET, is obtained for a tunnel FET with an $In_{0.53}Ga_{0.47}As$ (2.2 nm)/InAs (6.3 nm)/$In_{0.53}Ga_{0.47}As$ (94.4 nm) QW structure. It is found that the InAs QW tunnel FETs with the InAs QW thicker than 5 nm significantly degrade by high junction leakage current attributed to the lattice relaxation. *Published by AIP Publishing.* https://doi.org/10.1063/1.4992005

I. INTRODUCTION

The decrease in the subthreshold swing (S.S.) of Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) is mandatory for supply voltage scaling without an increase in leakage current. However, it is well-known that MOSFETs have the S.S. limitation of 60 mV/dec at room temperature because the thermal injection current of MOSFETs in the subthreshold region is dominated by Fermi Dirac statistics.

As a result of this fact, a tunnel Field Effect Transistor (tunnel FET) using band-to-band tunneling has attracted interest as a low power transistor. This is because tunnel FETs have potential to achieve S.S. steeper than 60 mV/dec, which is the lower limitation of S.S. of MOSFETs at room temperature.[1–3] Actually, Si-based tunnel FETs have been reported to exhibit S.S. values lower than 60 mV/dec.[4–6] However, one of the disadvantages of Si-based tunnel FETs is much lower on-current (I_{on}) than that of MOSFETs. This low I_{on} originates from the large and indirect bandgap, resulting in low tunneling probability. Therefore, III-V compound semiconductor materials are being expected as channel materials of tunnel FETs to provide much higher I_{on} than Si because of their narrow and direct bandgap.[7–17]

Among a variety of III-V compound semiconductor materials, $In_{0.53}Ga_{0.47}As$ lattice-matched on InP is one of the most promising materials for tunnel FET applications because of the comparably good property of the MOS interfaces. Many tunnel FETs based on III-V materials have been fabricated particularly with type-II heterojunctions such as GaAsSb/InGaAs, which can decrease the effective bandgap for further enhancing the tunneling current.[10–12] These type-II heterojunction tunnel FETs have been often fabricated using vertical tunnel structures. A $GaAs_{0.4}Sb_{0.6}/In_{0.65}Ga_{0.35}As$ heterojunction tunnel FET has been demonstrated with a large I_{on} of 275 $\mu A/\mu m$ and a S.S. value of less than 60 mV/dec at $V_{DS} = 0.5$ V and $V_G = 1.5$ V under the pulse I-V measurement condition.[10] Also, an InAs/GaAsSb/GaSb heterojunction tunnel FET has achieved the minimum S.S. ($S.S._{min}$) of 48 mV at $V_{DS} = 0.1$ V and an I_{on} value of 10.6 $\mu A/\mu m$ at $V_{DD} = 0.3$ V and $I_{off} = 1$ nA.[12] However, the vertical structure of the type-II heterojunction tunnel FET including a side wall channel defined by an epitaxial growth process is not necessarily compatible with the standard CMOS technology.

On the other hand, a planar type InGaAs tunnel FET has attracted strong interest because of the simpler structure and the CMOS process compatibility.[13–17] Here, high source doping concentrations (P^+ for n-channel tunnel FETs) and steep impurity profiles in the source junction are mandatory for reducing the depletion layer thickness of the p-n junctions,

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which determines the tunneling distance.[1,2] Zn is one of the most favorable impurities to form p^+ regions in InGaAs at concentrations higher than $1 \times 10^{19}\,cm^{-3}$ with the steep profiles.[15–21] It has been reported that the diffusion coefficient of Zn in InGaAs is proportional to the square of the Zn concentration.[15,19–21] Because of this inherent property of Zn diffusion in InGaAs, the extremely steep profile of 3.5 mV/dec has been realized by solid phase Zn diffusion.[15] A planar type InGaAs Tunnel FET with the Zn diffused source achieved a large I_{on}/I_{off} ratio over 10^6 and a $S.S._{min}$ value of 64 mV/dec at 3-nm-thick Al_2O_3 (EOT = 1.4 nm).[17] An EOT scaled InGaAs tunnel FET with the Zn-diffused source has exhibited a $S.S._{min}$ value of 54 mV/dec with a 2-nm-thick HfO_2/1-nm-thick Al_2O_3 (EOT = 0.8 nm) gate stack.[16]

For further performance improvement of the planar type InGaAs tunnel FET, the increase in the In content of $In_xGa_{1-x}As$ channels is effective because tunneling probability can be enhanced by the small bandgap.[15,16] A planar type InGaAs tunnel FET using an $In_{0.7}Ga_{0.3}As$ channel has improved the performance, resulting in the $S.S._{min}$ value of 60 mV/dec and higher I_{on} than those of the $In_{0.53}Ga_{0.47}As$ tunnel FET with 3-nm-thick HfO_2/1-nm-thick Al_2O_3 (EOT = 1.5 nm).[16] However, the reported high-In-content $In_xGa_{1-x}As$ tunnel FET shows not only high I_{on} but also large leakage current caused by the source junctions formed in the narrower bandgap material.[15,16]

II. DESIGN OF THE $In_xGa_{1-x}As$ QUANTUM WELL

Figure 1 shows the schematic structure of an ultra-thin $In_{0.53}Ga_{0.47}As$/$In_xGa_{1-x}As$ (y nm)/$In_{0.53}Ga_{0.47}As$ (97-y nm) Quantum Well (y-nm-thick $In_xGa_{1-x}As$ QW) tunnel FET proposed in this study. Here, the higher-In-content $In_xGa_{1-x}As$ QW layer is expected to provide higher tunneling probability, resulting in higher I_{on} due to the smaller bandgap than that of the single $In_{0.53}Ga_{0.47}As$ channel. On the other hand, the junction leakage current leading to high I_{off} can be suppressed by the junction formation inside $In_{0.53}Ga_{0.47}As$ regions with the larger bandgap in comparison to the higher-In-content $In_xGa_{1-x}As$ single channel. It is expected, therefore, that high I_{on} and low I_{off} can be simultaneously realized in the higher-In-content $In_xGa_{1-x}As$ QW channel tunnel FETs. It should be noted that the 3-nm-thick $In_{0.53}Ga_{0.47}As$ layer was epitaxially grown as a top layer to protect the high-In-content $In_xGa_{1-x}As$ quantum well layer from the loss due to surface oxidation and wet-chemical surface treatment during the tunnel FET fabrication process.

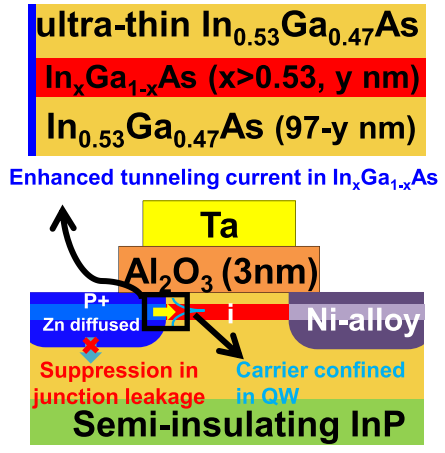

FIG. 1. Schematic structure of an $In_xGa_{1-x}As$ tunnel FET with a higher-In-content QW channel, which holds an advantage to enhance the tunneling current without any increase in the junction leakage current.

One of the most important parameters as the channel design of the $In_xGa_{1-x}As$ QW tunnel FET is the effective bandgap of the higher-In-content $In_xGa_{1-x}As$ QW layers because electron tunneling induced by gate voltage in the structure, shown in Fig. 1, is expected to occur from the valence band of the higher-In-content $In_xGa_{1-x}As$ QW layer to the conduction band. Here, the effective bandgap in the $In_xGa_{1-x}As$ QW layers is dependent on the In content (x), the QW thickness (y), and strain in the QW layers. The bandgap of unstrained $In_xGa_{1-x}As$ becomes smaller with an increase in the In content (x).[22] On the other hand, compressive strain caused by lattice mismatch between the high-In-content $In_xGa_{1-x}As$ QW layer and $In_{0.53}Ga_{0.47}As$ induces shifts of the conduction and valence band edges of $In_xGa_{1-x}As$, resulting in a small increase in the bandgap of $In_xGa_{1-x}As$ QW.[23–25] In addition, the QW thickness (y) less than around 10 nm lifts up the conduction band edge of the $In_xGa_{1-x}As$ QW layer and lowers the valance band edge due to the quantum size effect,[23,26,27] resulting in an increase in the bandgap.

Therefore, the effective bandgap [$E_{geff}(x,y)$] of the $In_xGa_{1-x}As$ QW layers, which determines inter-band electron tunneling in the $In_xGa_{1-x}As$ QW from the heavy hole band to the conduction band, is represented in the following equation, as shown in Fig. 2:

$$E_{geff}(x,y) = E_g(x) + \delta E_c(x) - \delta E_v(x) + E_{1E}(x,y) + E_{1HH}(x,y). \quad (1)$$

Here, $E_g(x)$, $\delta E_c(x)$, and $\delta E_v(x)$ mean the energy bandgap, the conduction band shift by biaxial compressive strain, and the valence band shift by biaxial compressive strain of $In_xGa_{1-x}As$ as a function of the In content (x), respectively. Also, $E_{1E}(x, y)$ and $E_{1HH}(x, y)$ are the lowest sub-band energies (n = 1) of electrons in the conduction band and the lowest sub-band energy (n = 1) of heavy holes in the valence band of $In_xGa_{1-x}As$ as the functions of the In content (x) and the QW thickness (y), respectively. The amounts of $\delta E_c(x)$ and $\delta E_v(x)$ are given by the following equations:[23–25]

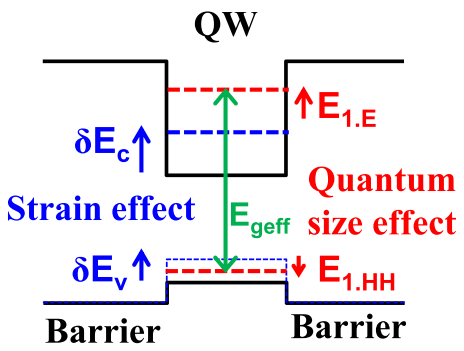

FIG. 2. Schematic diagram for the effective bandgap of the $In_xGa_{1-x}As$ QW. The compressive strain and the quantum confinement effect change the effective bandgap of the $In_xGa_{1-x}As$ QW.

$$\delta E_c = 2a_c \frac{C_{12}-C_{11}}{C_{11}}\varepsilon, \quad (2)$$

$$\delta E_v = 2a_v \frac{C_{12}-C_{12}}{C_{12}}\varepsilon - b\frac{C_{12}+C_{11}}{C_{11}}\varepsilon. \quad (3)$$

Here, a_c and a_v are the hydrostatic deformation potentials for the conduction band and the valence band, respectively. Also, b, C, and ε are the shear deformation potential, the elastic constant, the strain of $In_xGa_{1-x}As$, respectively. The calculation parameters are taken from the values given in Ref. 22.

$\delta E_c(x)$ and $\delta E_v(x)$ by biaxial compressive strain of the $In_xGa_{1-x}As$ layer rarely increase the effective bandgap because the energy of the heavy hole band moves upward.[24] It should be noted, however, that this strain effect also affects the conduction band offset (CBO) and valence band offset (VBO) between the $In_{0.53}Ga_{0.47}As$ barrier layer and the $In_xGa_{1-x}As$ QW layer, which affects $E_{1E}(x,y)$ and $E_{1HH}(x,y)$ through the penetration of the wave function into the $In_{0.53}Ga_{0.47}As$ barrier layer.

$E_{1E}(x,y)$ and $E_{1HH}(x,y)$, determined by the quantum size effect in the $In_{0.53}Ga_{0.47}As/In_xGa_{1-x}As$ (y nm)$/In_{0.53}Ga_{0.47}As$ quantum well on an InP substrate, are calculated as the functions of the In content (x) and the QW thickness (y) by solving the Schrodinger equation with consideration of the In-content-dependent effective carrier mass m* of $In_xGa_{1-x}As$. The heavy hole mass is used for the $E_{1HH}(x,y)$ calculation. The solution of the Schrodinger equation for electrons using the border condition of $\psi_{QW}(y/2) = \psi_{barrier}(y/2)$ and $\psi'_{QW}(y/2)/m^*_{QW} = \psi'_{barrier}(y/2)/m^*_{barrier}$[28] is given by

$$\tan\left(\sqrt{2m^*_{QW}E_{1E}}\frac{\pi y}{h}\right) = \sqrt{\frac{m^*_{QW}}{m^*_{barrier}}\frac{CBO - E_{1E}}{E_{1E}}}. \quad (4)$$

The solution for E_{1HH} can be obtained by the same equation with VBO instead of CBO. The value of CBO and VBO in strained $In_xGa_{1-x}As$ is used for calculation. Unstrained CBO at $In_{0.53}Ga_{0.47}As/In_xGa_{1-x}As$ hetero-interfaces is determined by the interpolation value of unstrained $CBO_{In0.53Ga0.47As/InAs}$ between $In_{0.53}Ga_{0.47}As$ and InAs. Unstrained $CBO_{In0.53Ga0.47As/InAs}$ is extracted from the bandgap values of $In_{0.53}Ga_{0.47}As$, InAs, and InP and unstrained VBO values at $In_{0.53}Ga_{0.47}As/InP$ and InAs/InP hetero-interfaces.[22] $E_{1E}(y)$ and $E_{1H.H}(y)$ by the quantum size effect increase with a decrease in the $In_xGa_{1-x}As$ QW thickness. Therefore, thicker QWs are favorable for lowering the bandgap of the $In_xGa_{1-x}As$ QW and increasing the probability of band-to-band tunneling.

Figure 3 shows the calculated effective bandgap E_{geff} of the $In_xGa_{1-x}As$ QW as a function of the QW thickness (y), which affects the quantum size effect. The In content is the parameter, which affects the compressive strain. The effective bandgap E_{geff} of the $In_xGa_{1-x}As$ QW decreases with an increase in the In content (x) and the QW thickness (y). However, the QW thickness (y) of the high-In-content $In_xGa_{1-x}As$ QW is limited by the critical thickness which is defined as the maximum growth thickness without lattice relaxation. When the lattice of an $In_xGa_{1-x}As$ QW layer is relaxed by the lattice mismatch with that of the barrier layer, a lot of dislocations and defects are generated in the $In_xGa_{1-x}As$ QW layer, leading to high I_{off} and S.S. Thus, the QW thickness (y) of high-In-content $In_xGa_{1-x}As$ has to be thinner than the critical thickness.

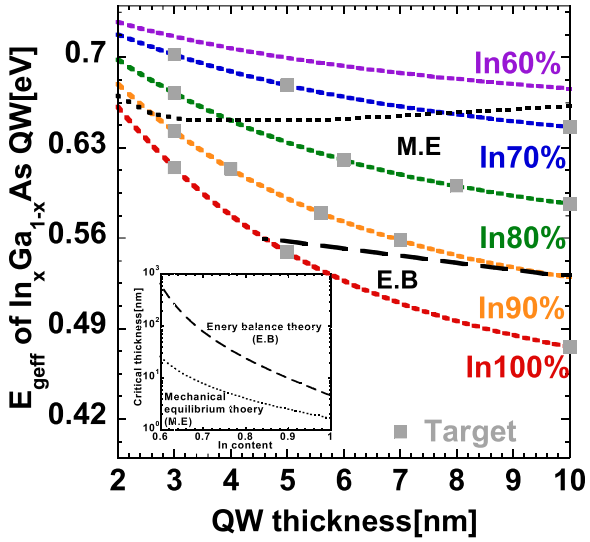

FIG. 3. Effective bandgap E_{geff} of the $In_xGa_{1-x}As$ QW versus the well thickness. The critical thickness based on the Mechanical Equilibrium model (M.E.)[31] and the Energy balance model (E.B.)[32] is also given.

In order to estimate the critical thickness of the $In_xGa_{1-x}As$ QW, the mechanical equilibrium model[29] and the energy balance model[30] are introduced. The estimated critical thickness is shown as the dashed lines in Fig. 3. In the mechanical equilibrium model,[29] where the force exerted by the misfit strain is assumed to be identical to tension in dislocation lines, the critical thickness, h_{ME}, of $In_xGa_{1-x}As$ on $In_{0.53}Ga_{0.47}As$ in terms of generating the misfit 60° type of dislocation is given by

$$h_{ME} = \frac{b}{4\pi\varepsilon}\frac{1-\frac{v}{4}}{1+v}\left(ln\frac{h_{ME}}{b}+1\right), \quad (5)$$

where b, ε, and v, are the Burgers vector, strain, and Poisson ratio, respectively.

Meanwhile, the energy balance model suggests that when the areal strain energy density is equal to the energy density of screw, edge, and half-loop dislocations, the critical thickness, h_{EB}, of $In_xGa_{1-x}As$ on $In_{0.53}Ga_{0.47}As$ is determined by the following equation:[30]

$$h_{EB} = \frac{1}{16\sqrt{2}\pi}\frac{b^2}{a(x)}\frac{1-v}{1+v}\frac{1}{\varepsilon^2}\ln\left(\frac{h_{EB}}{b}\right), \quad (6)$$

where a(x) is the lattice constant of $In_xGa_{1-x}As$.

The critical thickness of $In_xGa_{1-x}As$ on $In_{0.53}Ga_{0.37}As$ calculated from the following two models is also plotted in Fig. 3. On the other hand, the reliable experimental data of the critical thickness of high-In-content $In_xGa_{1-x}As$ layers grown on $In_{0.53}Ga_{0.47}As$ have not reported yet. Here, it is expected that the critical thickness of $In_xGa_{1-x}As$ on $In_{0.53}Ga_{0.47}As$ is a value between the above two models. The critical thickness of $In_xGa_{1-x}As$ by both models decreases

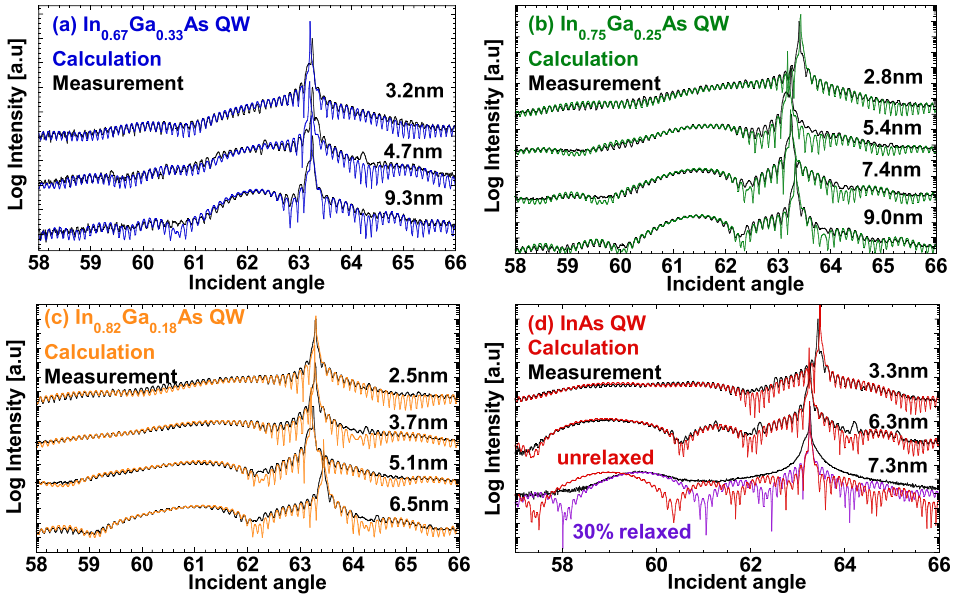

FIG. 4. X-ray diffraction (XRD) spectra of the $In_xGa_{1-x}As$ QW designed with the In contents of (a) 70%, (b) 80%, (c) 90%, and (d) 100%. The extended rocking curve analysis (a)–(d) shows the In content of 67% and the QW thicknesses of 3.2, 4.7, and 9.3 nm, the In content of 75% and the QW thicknesses of 2.8, 5.4, 7.4, and 9 nm, the In content of 82% and the QW thicknesses of 2.5, 3.7, 5.1, and 6.5 nm, and the In content of 100% and the QW thicknesses of 3.3, 6.3, and 7.3 nm, respectively. The 7.3 nm-thick-InAs layer is relaxed with the relaxation ratio of around 30%.

with an increase in the In content, while the E_{geff} of the $In_xGa_{1-x}As$ QW increases with a decrease in the QW thickness (y) because of the quantum size effect. Thus, the In content (x) and QW thickness (y) of the $In_xGa_{1-x}As$ QW should be optimized for minimizing their effective bandgap E_{geff} under the condition of no lattice relaxation. On the other hand, the lattice relaxation of the QW could be dependent on the epitaxial growth conditions. Therefore, we prepared a wide variety of $In_xGa_{1-x}As$ QWs with different In contents (x) and QW thicknesses (y) in order to minimize E_{geff} under the QW layers thicker than the critical thickness, as shown in Fig. 3. We also evaluated the physical properties of the QW layers and the performance of tunnel FETs using the QW structures. Here, the In content of $In_xGa_{1-x}As$ was changed among 70%, 80%, 90%, and 100% as the nominal values, and the nominal QW thickness (y) of $In_xGa_{1-x}As$ was varied from 3 nm to 10 nm as shown in Fig. 3. Note here that most of the $In_xGa_{1-x}As$ QWs are expected to have the thickness intermediate between the critical thickness determined by the mechanical equilibrium model and the energy balance model.

III. EVALUATION OF THE $In_xGa_{1-x}As$ QUANTUM WELL

$In_{0.53}Ga_{0.47}As$ (3 nm)/$In_xGa_{1-x}As$ (y nm)/$In_{0.53}Ga_{0.47}As$ (97-y nm) QWs, named y-nm-thick $In_xGa_{1-x}As$ QWs, with different In contents (x) and QW thicknesses (y) were grown on semi-insulating InP substrates by Metal-organic Vapor Phase Epitxay (MOVPE). The real In content (x) and QW thickness (y nm) of $In_xGa_{1-x}As$ QWs were estimated using X-ray diffraction (XRD) spectra. Figure 4 shows the XRD spectra of $In_xGa_{1-x}As$ QWs with different In contents. Here, the In content and the QW thickness were determined by fitting of the experimental spectra with the simulation ones. As a result, the In content of the $In_xGa_{1-x}As$ QW with the nominal In contents of 70%, 80%, 90%, and 100% was estimated to be 67%, 75%, 82%, and 100%, respectively. The error range of the $In_xGa_{1-x}As$ QW thickness obtained from the XRD measurement results is estimated to be thinner than 1 nm, except for 6.3- and 7.3-nm-thick InAs QWs. The 7.3-nm-thick InAs QW showed the lattice relaxation by around 30%, while the samples in the other conditions exhibited no lattice relaxation. The evaluated In contents and QW thicknesses of the $In_xGa_{1-x}As$ QW grown by MOVPE for tunnel FET fabrication are summarized in Table I.

TABLE I. In content and QW thickness of the $In_xGa_{1-x}As$ QW determined from the XRD spectra analysis.

In content (x)	QW thickness (y)
67%	3.2 nm, 4.7 nm, 9.3 nm
75%	2.8 nm, 5.4 nm, 7.4 nm, 9.0 nm
82%	2.5 nm, 3.7 nm, 5.1 nm, 6.5 nm
100%	3.3 nm, 6.3 nm, 7.3 nm

The photoluminescence of the $In_xGa_{1-x}As$ QW was measured to evaluate E_{geff}. Figure 5 shows an example of the PL spectra of the $In_{0.75}Ga_{0.25}As$ QW at room temperature. Here,

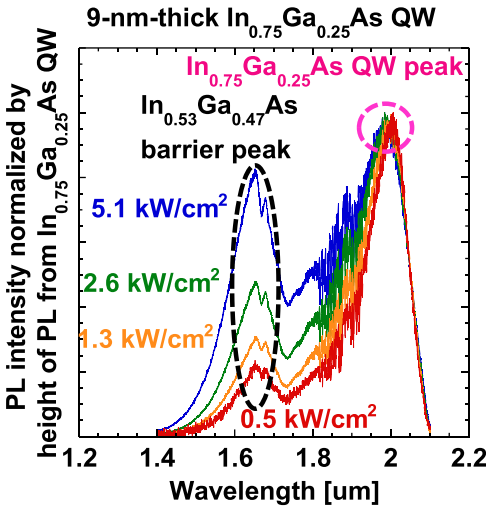

FIG. 5. The photoluminescence (PL) measurement of the $In_xGa_{1-x}As$ QW at room temperature. Laser power is controlled to estimate the $In_xGa_{1-x}As$ QW peak.

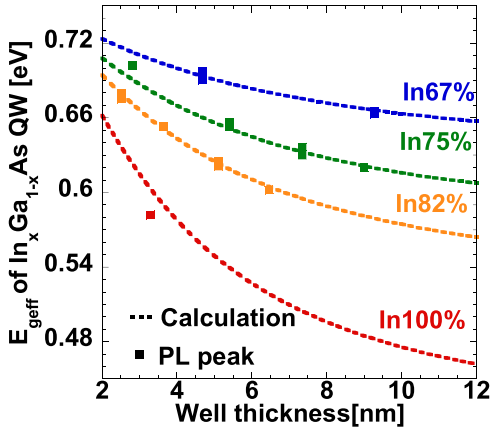

FIG. 6. Bandgap of the $In_xGa_{1-x}As$ QW estimated by the PL peaks and the XRD spectra. The calculated bandgap is in good agreement with the results from the PL peaks.

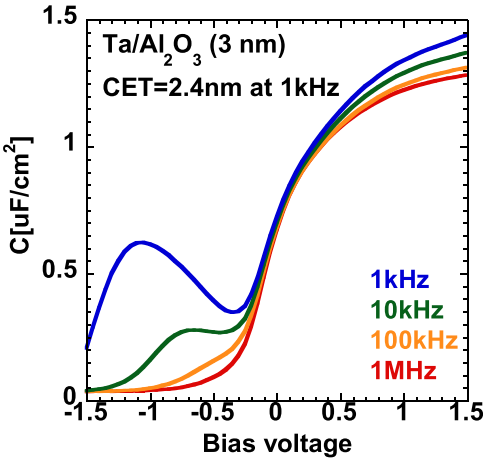

FIG. 8. C-V characteristics of a Ta (17 nm)/Al_2O_3(3 nm) InGaAs MOS capacitor. The CET of the Ta (17 nm)/Al_2O_3(3 nm) gate stack amounts to 2.4 nm.

the PL data were normalized by the peak height of PL from the $In_{0.75}Ga_{0.25}As$ QW layer. The intensity of the QW peak increases relatively with a decrease in the power density of an exciting laser, and we have confirmed that the total PL intensity decreases with the decreasing power density. This fact can be explained by considering that the lower power density causes the larger reduction of the excited electrons density in the $In_{0.53}Ga_{0.47}As$ QW than in the $In_xGa_{1-x}As$ QW layer. The laser power lower than 500 W/cm^2 is sufficient to estimate the $In_xGa_{1-x}As$ QW peaks. Also, an extended InGaAs photo diode detector was used for measuring $In_xGa_{1-x}As$ QW peaks with the short wavelength. On the other hand, the PL peak of the $In_{0.67}Ga_{0.33}As$ QW with the QW thickness of 3.2 nm could not be identified because of the much weaker PL intensity than the $In_{0.53}Ga_{0.47}As$ PL peak. Also, the PL peaks of 6.3- and 7.3-nm-thick InAs QWs could not be obtained because of the limitation in the measurement range of the extended InGaAs detector.

Figure 6 shows the E_{geff} values of the $In_xGa_{1-x}As$ QW estimated from the PL peak wavelength and the calculated bandgap of the $In_xGa_{1-x}As$ QW. The values of the In content (x) and the QW thickness (y) of the $In_xGa_{1-x}As$ QW estimated from the XRD spectra were used to calculate E_{geff} shown in Fig. 6. The experimental E_{geff} of the $In_xGa_{1-x}As$ QW evaluated by PL peaks shows good agreement with the calculated one based on the values of the In content and the QW thickness obtained from the XRD spectra.

IV. DEVICE FABRICATION

The fabrication flow of a planar-type InGaAs QW tunnel FET is shown in Fig. 7. The $In_xGa_{1-x}As$ QWs grown by MOVPE were cleaned with acetone and NH_4OH. By the atomic layer deposition method (ALD), 10-nm-thick Al_2O_3 was deposited as a diffusion mask at 200 °C. Next, the Al_2O_3 layer on the source area was etched using a buffered HF solution for selective Zn diffusion. Subsequently, samples were baked for 30 min in air to eliminate moisture on the surface, and Zn-doped spin-on glass (SOG) was coated immediately with a spin coater under 3750 rpm. The Zn-doped SOG film was cured at 200 °C. By rapid thermal annealing (RTA) at 500 °C, Zn was driven for 60 s in a N_2 ambient furnace. The Zn-doped SOG film and the Al_2O_3 mask layer were removed using a diluted HF solution. Next, each device was isolated by etching InGaAs selectively with a mixture solution of H_3PO_4, H_2O_2, and H_2O. After surface pretreatment using acetone, NH_4OH, and $(NH_4)S_x$, 3-nm-thick Al_2O_3 by ALD at 200 °C and 17-nm-thick Ta by metal sputtering were deposited successively. By reactive ion etching (RIE) with the CF_4 plasma, Ta was etched selectively for gate formation. Post metal annealing (PMA) was performed by RTA at 350 °C for 10 s in a N_2 ambient furnace. Figure 8 shows the capacitance-voltage (C-V) characteristics of a Ta (17 nm)/Al_2O_3(3 nm) InGaAs MOS capacitor. This gate stack exhibited a capacitance equivalent thickness (CET) of 2.4 nm. Subsequently, 20 nm thick Ni was deposited on the drain

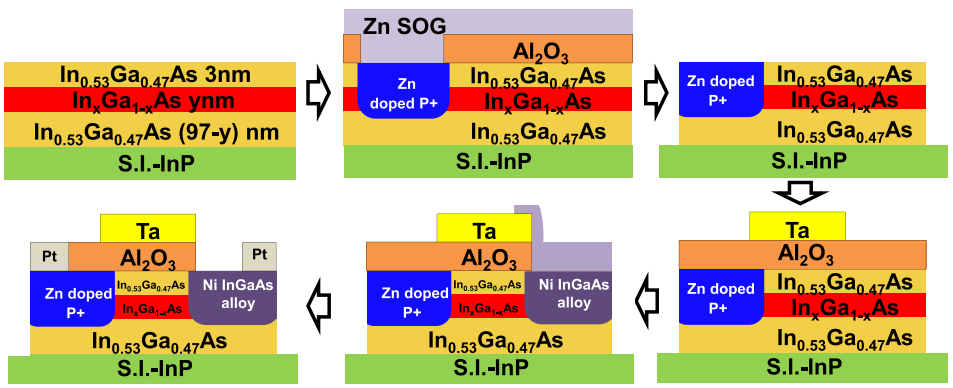

FIG. 7. Process flow of an $In_xGa_{1-x}As$ QW tunnel FET. Zn diffusion was used for source junction formation in order to realize defect-less p^+/n junctions with steep Zn profiles.

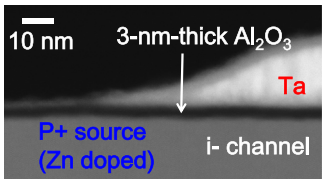

FIG. 9. TEM image of the $In_{0.82}Ga_{0.18}As$ QW tunnel FET.

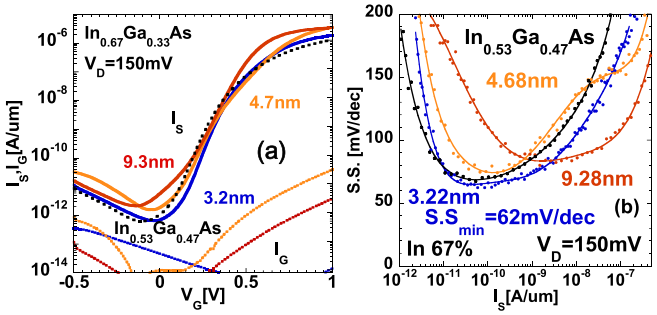

FIG. 10. (a) I_S-V_G curves and (b) the S.S.-I_S characteristics of the $In_{0.67}Ga_{0.33}As$ QW tunnel FETs and the control $In_{0.53}Ga_{0.47}As$ tunnel FET.

regions by electron-beam thermal evaporation. The Ni-InGaAs alloy was formed by RTA at 250 °C for 60 s in a N_2 ambient furnace.[31] Unreacted Ni was removed selectively using a diluted HCl solution. Finally, Pt contact pads were deposited by a liftoff process. The control $In_{0.53}Ga_{0.47}As$ tunnel FETs were also fabricated by the same process. Figure 9 shows a transmission electron microscopy (TEM) image near a source/channel region of a fabricated $In_{0.82}Ga_{0.18}As$ QW tunnel FET. It is confirmed that the flat MOS interface is formed.

V. ELECTRICAL CHARACTERISTICS OF THE FABRICATED $In_xGa_{1-x}As$ QUANTUM WELL TUNNEL FET

$In_xGa_{1-x}As$ QW tunnel FETs were fabricated and operated for all the In content QWs. It is shown that the gate leakage current (I_G) of the $In_xGa_{1-x}As$ QW tunnel FETs is low enough to be neglected, meaning that the source current (I_S) is nearly the same as the drain current (I_D). The I_S-V_G characteristics of the control $In_{0.53}Ga_{0.47}As$ tunnel FET are included in each figure of those of the $In_xGa_{1-x}As$ QW tunnel FETs for comparison. Here, I_{on} and I_{off} are defined as the maximum current and the minimum current, respectively, in a V_G range of −0.5 V–1 V.

Figures 10(a) and 10(b) show the I_S-V_G and S.S.-I_S characteristics, respectively, of $In_{0.67}Ga_{0.33}As$ QW tunnel FETs with the QW thicknesses of 3.2, 4.7, and 9.3 nm at V_D=150 mV. I_{on} in the $In_{0.67}Ga_{0.33}As$ QW tunnel FETs is found to increase with the increasing QW thickness. The I_{on} of $In_{0.67}Ga_{0.33}As$ QW tunnel FETs with the QW thicknesses of 3.2, 4.7, and 9.3 nm is 1.9, 3.5, and 3.5 $\mu A/\mu m$, respectively, higher than the I_{on} of 1.3 $\mu A/\mu m$ of the control $In_{0.53}Ga_{0.47}As$ tunnel FET. Also, the I_{off} of $In_{0.67}Ga_{0.73}As$ QW tunnel FETs is significantly lower than that of the $In_{0.7}Ga_{0.3}As$ single-channel tunnel FET, reported in Ref. 15. On the other hand, it is observed that I_{off} slightly increases with the increasing QW thickness, resulting in the degradation of the S.S. characteristics. This I_{off} increase can be related to the generation of any defects and dislocations in thicker $In_{0.67}Ga_{0.33}As$ QWs, which can weaken the gate controllability over the current. We also evaluated the surface roughness of the $In_{0.67}Ga_{0.33}As$ QW using an atomic force microscope (AMF). Figures 11(a)–11(c) show the AFM images of the $In_{0.67}Ga_{0.33}As$ QW with the QW thicknesses of 3.2, 4.7, and 9.3 nm, respectively. It is found that the root means square (RMS) of the surface roughness of the $In_{0.67}Ga_{0.33}As$ QW slightly increases with an increase in the QW thickness. This result suggests that the density of defects and dislocations in the $In_{0.67}Ga_{0.33}As$ layers can start to increase with an increase in the $In_{0.67}Ga_{0.33}As$ thickness, even though the thickness of $In_{0.67}Ga_{0.33}As$ does not reach the critical thickness.

The 3.2-nm-thick $In_{0.67}Ga_{0.33}As$ QW tunnel FET with the RMS of 0.14 nm, which is sufficiently flat in comparison to the RMS of 0.16 nm of the control $In_{0.53}Ga_{0.47}As$, exhibits slightly steeper S.S. characteristics than the control $In_{0.53}Ga_{0.47}As$ tunnel FET. The minimum value of S.S. ($S.S._{min}$) of 62 mV/dec is achieved with the 3.2-nm-thick $In_{0.67}Ga_{0.33}As$ QW tunnel FET, as shown in Fig. 10(b). The $In_{0.67}Ga_{0.33}As$ QW tunnel FETs with the QW thicknesses of 4.7 and 9.3 nm exhibit the degraded S.S. characteristics in a low I_S range because of an increase in I_{off} possibly due to the generation of defects and dislocation. On the other hand, the S.S. characteristics of the 9.3-nm-thick $In_{0.67}Ga_{0.33}As$ QW tunnel FET is better in the I_S range higher than 10^{-9} $\mu A/\mu m$ than those of the control $In_{0.53}Ga_{0.47}As$ tunnel FET, which is attributable to the enhanced tunneling current by the narrower bandgap of the $In_{0.67}Ga_{0.33}As$ QW.

Figures 12(a) and 12(b) show the I_S-V_G and the S.S.-I_S characteristics, respectively, of the $In_{0.75}Ga_{0.25}As$ QW tunnel FETs with the QW thicknesses of 2.8, 5.4, 7.4, and 9 nm at V_D=150 mV. The higher I_{on} values of 2.1, 4.6, 4.1, and 4.3 $\mu A/\mu m$ are achieved by the $In_{0.75}Ga_{0.25}As$ QW tunnel FETs with the QW thicknesses of 2.8, 5.4, 7.4, and 9 nm, respectively. However, the $In_{0.75}Ga_{0.25}As$ QW tunnel FETs with

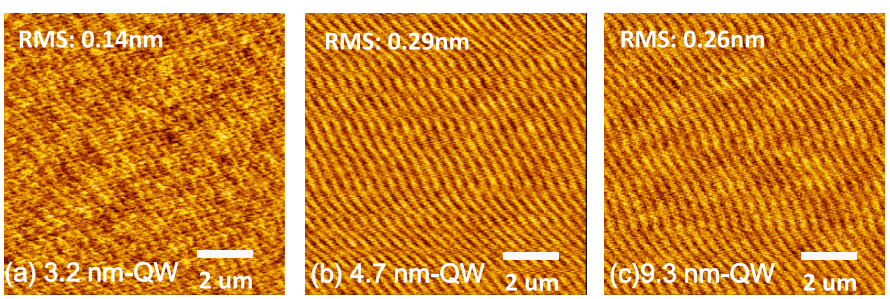

FIG. 11. AFM images of $In_{0.67}Ga_{0.33}As$ QW surfaces: (a) 3.2-nm-thick $In_{0.67}Ga_{0.33}As$ QW, (b) 4.7-nm-thick $In_{0.67}Ga_{0.33}As$ QW, and (c) 9.3-nm-thick $In_{0.67}Ga_{0.33}As$ QW.

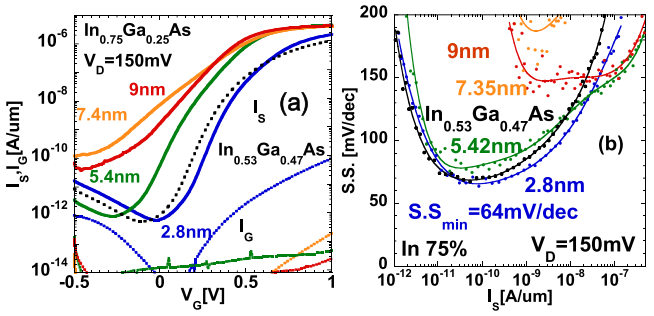

FIG. 12. (a) I_S-V_G curves and (b) the S.S.-I_S characteristics of the $In_{0.75}Ga_{0.25}As$ QW tunnel FET and the control $In_{0.53}Ga_{0.47}As$ tunnel FET.

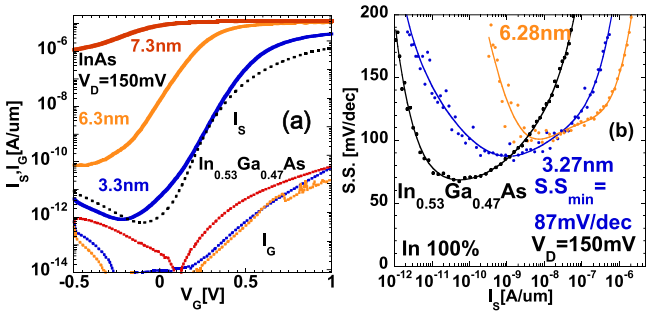

FIG. 14. (a) I_S-V_G curves and (b) the S.S.-I_S characteristics of the InAs QW Tunnel FET and the control $In_{0.53}Ga_{0.47}As$ Tunnel FET.

the QW thicknesses of 7.4 and 9 nm show a significant increase in I_{off}, while the other $In_{0.75}Ga_{0.25}As$ QW tunnel FETs with the QW thicknesses of 2.8 and 5.4 nm exhibit a similar I_{off} value to that of the control $In_{0.53}Ga_{0.47}As$ tunnel FET. This large increase in I_{off} of the $In_{0.75}Ga_{0.25}As$ QW tunnel FETs with the thicker QW thickness might be attributed to the increase in the densities of dislocations and defects in the $In_{0.75}Ga_{0.25}As$ layers on $In_{0.53}Ga_{0.47}As$. The 2.8-nm-thick $In_{0.75}Ga_{0.25}As$ QW tunnel FET exhibits a $S.S._{min}$ value of 64 mV/dec, as shown in Fig. 12(b), which is the slightly steeper S.S. characteristic than that of the control $In_{0.53}Ga_{0.47}As$ tunnel FET. On the other hand, the S.S. characteristics of the $In_{0.75}Ga_{0.25}As$ QW tunnel FETs with the QW thicknesses of 7.4 and 9 nm are degraded because of the large leakage current caused in the $In_{0.75}Ga_{0.25}As$ layers.

Figures 13(a) and 13(b) show the I_S-V_G characteristics and the S.S.-I_S characteristics, respectively, of the $In_{0.82}Ga_{0.18}As$ QW tunnel FETs with the QW thicknesses of 2.5, 3.7, 5.1, and 6.5 nm at V_D=150 mV. The I_{on} of the $In_{0.82}Ga_{0.18}As$ QW tunnel FETs with the QW thicknesses of 2.5, 3.7, 5.1, and 6.5 nm amounts to 1.3, 1.6, 2.7, and 3.6 $\mu A/\mu m$, respectively. While the $In_{0.82}Ga_{0.18}As$ QW tunnel FETs with the QW thicknesses of 2.5, 3.7, and 5.1 nm exhibit lower I_{off} than the control $In_{0.53}Ga_{0.47}As$ tunnel FET, I_{off} is higher in the 6.5-nm-thick $In_{0.82}Ga_{0.18}As$ QW tunnel FET. The 2.5-nm-thick $In_{0.82}Ga_{0.18}As$ QW tunnel FET exhibits the steeper S.S. characteristics with the $S.S._{min}$ of 63 mV/dec than the control $In_{0.53}Ga_{0.47}As$ tunnel FET. Also, the 6.5-nm-thick $In_{0.82}Ga_{0.18}As$ QW tunnel FET exhibits less steeper S.S. characteristics in a low I_S range because of increased I_{off}, while it shows the improved S.S. characteristics in I_S higher than 5×10^{-9} $\mu A/\mu m$ because of the enhanced tunneling current.

Figures 14(a) and 14(b) show the I_S-V_G and the S.S.-I_s characteristics of the InAs QW tunnel FETs at V_D=150 mV. The InAs QW tunnel FETs achieve the best improvement of I_{on} among the fabricated $In_xGa_{1-x}As$ QW tunnel FETs because of the comparatively low bandgap. The I_{on} of the InAs QW tunnel FETs with the QW thicknesses of 3.3, 6.3, and 7.3 nm amounts to 4.2, 11, and 12 $\mu A/\mu m$, respectively, which are 3.3, 8.5, and 9.2 times higher than those of 1.3 $\mu A/\mu m$ in the control $In_{0.53}Ga_{0.47}As$ tunnel FET. However, the I_S of the 7.3-nm-thick InAs QW tunnel FET is rarely controlled by V_G. The clear increase in I_{off} with an increase in the QW thickness is attributable to lattice relaxation of InAs, which can generate lots of defects and dislocations. On the other hand, the I_{off} of the 3.3-nm-thick InAs tunnel FET is as low as that of the control $In_{0.53}Ga_{0.47}As$ tunnel FET. However, the gate controllability of the 3.3-nm-thick InAs tunnel FET becomes weaker in a lower I_S region than that of the control $In_{0.53}Ga_{0.47}As$ tunnel FET, and this causes the $S.S._{min}$ of 84 mV/dec higher than 66 mV/dec of the control $In_{0.53}Ga_{0.47}As$ tunnel FET. These results may be related to the larger surface roughness of InAs, attributable to large compressive strain in the InAs QW layer. The InAs QW tunnel FETs with the QW thicknesses of 6.3 and 7.3 nm exhibit degraded S.S. characteristics because of the large I_{off}. However, the S.S. characteristics of InAs tunnel FETs with the QW thicknesses of 3.3 and 6.3 nm are improved with I_S higher than 10^{-9} and 3×10^{-9} $\mu A/\mu m$, respectively.

Figures 15(a) and 15(b) summarize the I_{off} and $S.S._{min}$, respectively, of the $In_xGa_{1-x}As$ QW tunnel FETs with the In contents of 67, 75, 82, and 100% as a function of the QW thickness. It is found that the decrease in the QW thickness can lead to reduction in $S.S._{min}$, attributable to the

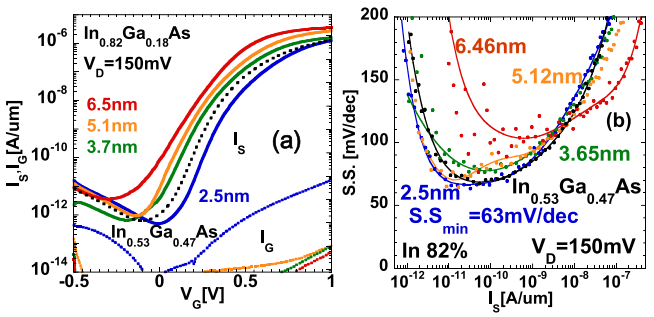

FIG. 13. (a) I_S-V_G curves and (b) the S.S.-I_S characteristics of the $In_{0.82}Ga_{0.18}As$ QW Tunnel FET and the control $In_{0.53}Ga_{0.47}As$ Tunnel FET.

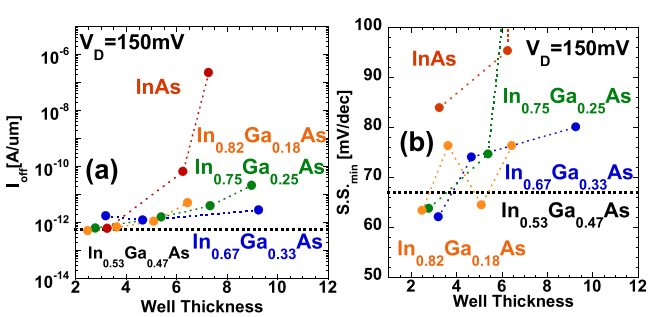

FIG. 15. (a) I_{off}-QW thickness relationship and (b) $S.S._{min}$-QW thickness relationship of $In_xGa_{1-x}As$ QW tunnel FETs as a parameter of the In content.

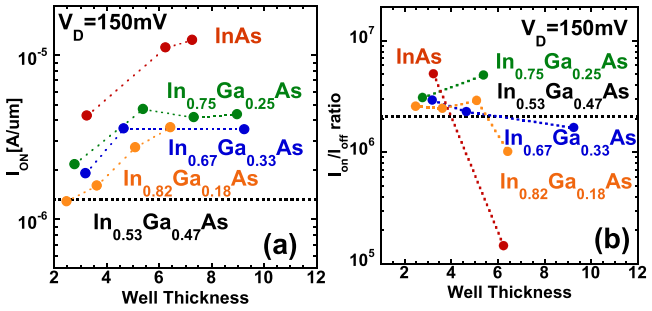

FIG. 16. (a) I_{on}-QW thickness relationship and (b) I_{on}/I_{off} ratio-QW thickness relationship of $In_xGa_{1-x}As$ QW tunnel FETs as a parameter of the In content.

suppression of the leakage current and better current control by V_G. Especially, the I_{off} of the $In_xGa_{1-x}As$ QW tunnel FETs with the QW thickness thinner than 5 nm is suppressed to the same level as in the control $In_{0.53}Ga_{0.47}As$ tunnel FET. This result can be explained by the suppression of generation of defects and dislocations due to lattice relaxation in the thinner QW thickness and resulting reduction of the increase in the junction leakage current.

Figures 16(a) and 16(b) also summarize the I_{on} and the I_{on}/I_{off} ratio, respectively, of the $In_xGa_{1-x}As$ QW tunnel FETs with the In contents of 67%, 75%, 82%, and 100% as a function of the QW thickness. The I_{on} of the $In_xGa_{1-x}As$ QW tunnel FET increases with an increase in the QW thickness or the In content attributed to the decrease in effective E_g of $In_xGa_{1-x}As$ QW, shown in Fig. 6. As a result, the InAs QW tunnel FET is the most effective for achieving higher I_{on}. On the other hand, the I_{on}/I_{off} ratio of the $In_xGa_{1-x}As$ QW tunnel FETs is improved by thinning the QW thickness because of the suppressed I_{off}. In addition, an increase in the In content enhances the I_{on}/I_{off} ratio under the condition that I_{off} is well suppressed. The 3.3-nm-thick InAs QW tunnel FET exhibits the best I_{on}/I_{off} ratio of 5×10^6, which is 2.5 times higher than 2×10^6 in the control $In_{0.53}Ga_{0.47}As$ tunnel FET.

Figure 17 shows the I_{on} of the $In_xGa_{1-x}As$ QW tunnel FETs with the In contents of 67, 75, 82, and 100% as a function of the effective bandgap of the $In_xGa_{1-x}As$ QW. The values of the bandgap are experimentally estimated from the PL peaks, except for $In_{0.67}Ga_{0.33}As$ with the QW thickness of

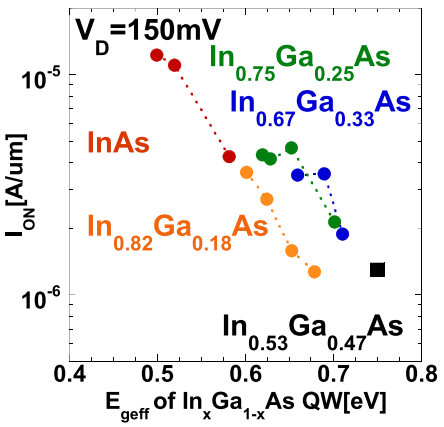

FIG. 17. I_{on} of $In_xGa_{1-x}As$ QW tunnel FETs as a parameter of the effective bandgap.

3.2 nm and the InAs QW with the thicknesses of 6.3 nm and 7.3 nm, where the calculated values are used because of the invisible PL peaks. It is confirmed that I_{on} increases with an increase in the bandgap of the QW layers. Here, we evaluated the Zn diffusion profiles with different In contents by SIMS analyses in order to examine the effects of the In content (x) of $In_xGa_{1-x}As$ on the Zn diffusion profiles, which can also contribute to the tunnel FET performance. The diffusion depth becomes deeper with the increasing In content (x). It is found, on the other hand, that the steepness of the Zn profiles and the maximum doping concentration are almost the same among different-In-content $In_xGa_{1-x}As$ QWs. This result indicates that the variation in the Zn profile among different In contents cannot be a main factor for the difference in the performance of tunnel FETs with different In contents. It is observed, on the other hand, that the I_{on} of the $In_{0.67}Ga_{0.33}As$ and $In_{0.75}Ga_{0.25}As$ QW tunnel FETs is higher than that of the $In_{0.82}Ga_{0.18}As$ QW tunnel FETs at the same E_{geff}, which seems to be inconsistent with the lower effective mass in the higher In-content InGaAs QW. One possible explanation for this result can be the larger interface state density at the MOS interfaces of the higher-In-content $In_xGa_{1-x}As$,[32] while further studies are still needed to identify the physical origin.

VI. PHYSICAL ORIGIN OF LEAKAGE CURRENT OF InAs QW TUNNEL FETs

In order to investigate a possible physical origin of the leakage current of the InAs QW tunnel FETs, the temperature dependence of the I_S-V_G characteristics of the InAs QW tunnel FETs with the QW thicknesses of 3.3, 6.3, and 7.3 nm and the control $In_{0.53}Ga_{0.47}As$ tunnel FET was measured. The measurement temperatures were varied from 200 to 340 K. Figure 18 shows the temperature dependence of the

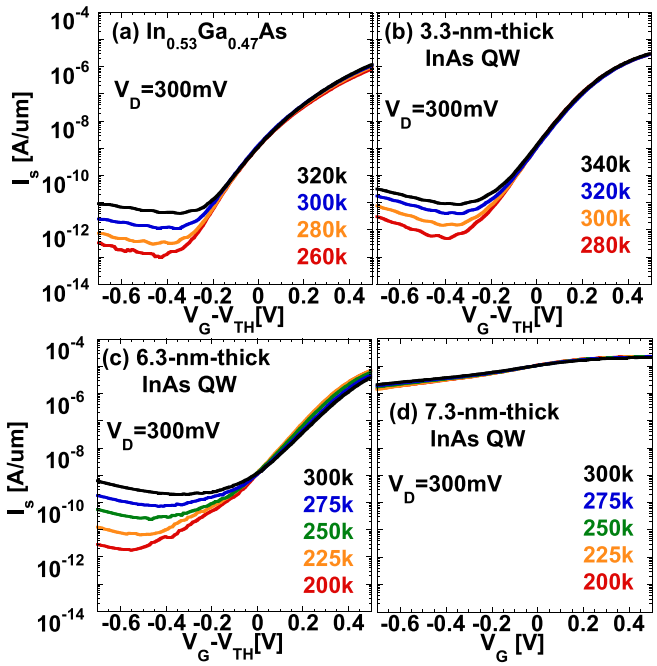

FIG. 18. Temperature dependence of the I_S-V_G characteristics of the InAs QW tunnel FETs with (a) the control $In_{0.53}Ga_{0.47}As$ tunnel FET and the QW thicknesses of (b) 3.3, (c) 6.3, and (d) 7.3 nm.

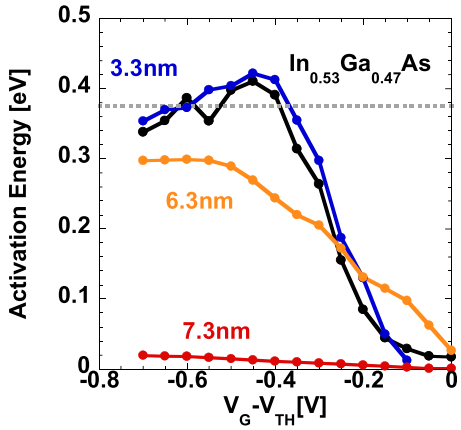

FIG. 19. Activation energy of the InAs QW tunnel FETs and the $In_{0.53}Ga_{0.47}As$ control tunnel FET. The 3.3-nm-thick InAs shows a similar activation energy curve to that of the control $In_{0.53}Ga_{0.47}As$ tunnel FET.

I_S-(V_G-V_{TH}) characteristics. Here, the threshold voltage V_{TH} is defined as V_G corresponding to the I_S of 10^{-9} μA/μm. It was found that the junction leakage current of the InAs QW tunnel FETs with the QW thicknesses of 3.3 and 6.3 nm and the control $In_{0.53}Ga_{0.47}As$ tunnel FET is decreased with the lowering measurement temperature. However, the I_S-V_G characteristics of the 7.3-nm-thick InAs QW tunnel FET are not dependent on temperature.

We estimated the activation energy of I_S at a V_D of 300 mV as a function of V_G-V_{TH} from the measured temperature dependence of the I_S-V_G characteristics in Fig. 18. Figure 19 shows the estimated activation energy. The activation energies of the 3.3-nm-thick InAs QW tunnel FET and the control $In_{0.53}Ga_{0.47}As$ tunnel FET in the off region are around 0.37 eV, which is approximately a half value of the $In_{0.53}Ga_{0.47}As$ bandgap energy. Thus, the leakage current of the 3.3-nm-thick InAs QW and the control $In_{0.53}Ga_{0.47}As$ tunnel FET is attributed to the generation/recombination (SRH) current related to bulk traps in the $In_{0.53}Ga_{0.47}As$ layers. This result indicates that the $In_xGa_{1-x}As$ QW structure is effective for suppressing an increase in the junction leakage current in high-In-content $In_xGa_{1-x}As$ layers. Meanwhile, the activation energies of the 7.3-nm-thick InAs QW tunnel FET are nearly 0 eV in the off region. This result suggests that the leakage current of the 7.3-nm-thick InAs QW tunnel FET can be caused by any non-thermal processes such as trap-assisted tunneling (TAT). The activation energy of the InAs QW tunnel FET with the QW thickness of 6.3 nm falls between the 3.3-nm-thick InAs QW and the 7.3-nm-thick InAs, indicating that the junction leakage current is determined by both a SRH process in the depletion regions of In0.53Ga0.47As and a non-thermal process such as TAT occurring at InAs/In0.53Ga0.47As and/or the MOS interfaces.

A possible physical origin of the TAT process is tunneling via defects in the bandgap of the InAs layers. Here, the defects and dislocations in InAs QW layers on $In_{0.53}Ga_{0.47}As$ can increase with an increase in the QW thickness because of the large lattice mismatch between InAs and $In_{0.53}Ga_{0.47}As$. Figure 20 shows the AFM images of the InAs QW with the QW thicknesses of 3.3, 6.3, and 7.3 nm. It is observed that the RMS values of the InAs QWs significantly increase with thickening QW layers, supporting an increase in the densities of defects and dislocations in the InAs QW with an increase in the thickness. The 3.3-nm-thick InAs QW exhibits the RMS value of 0.3 nm, which is still rougher than that of the 3.2-nm-thick $In_{0.67}Ga_{0.33}As$ QW (0.14 nm). This is attributable to much higher strain in the InAs QW than that of $In_{0.67}Ga_{0.33}As$. This large RMS of InAs may cause degradation of gate controllability in a lower I_S region, observed in Fig. 14.

It was also observed in the AFM images that there are grooves on the InAs QW with QW thicknesses of 6.3 and 7.3 nm. This fact can be an evidence of the lattice relaxation of the InAs QW layers with the QW thicknesses of 6.3 and 7.3 nm, which is consistent with the previous report that InAs on $In_{0.53}Ga_{0.47}As$ starts to be relaxed from 6 nm.[33] Here, the grooves are sparsely observed in the 6.3-nm-thick InAs QW. Also, the XRD results of the 6.3-nm-thick InAs QW suggest almost no relaxation. As a result, the 6.3-nm-thick InAs QW can be regarded as partially relaxed. The number of the grooves increases with an increase in the QW thickness. The XRD spectra of the 7.3-nm-thick InAs layer indicate the relaxation ratio of about 30%. Thus, we can consider that the relaxation ratio of the InAs layers increases with an increase in the InAs thickness.

It can be concluded from these electrical and physical analyses that defects and dislocations in the InAs and higher In-content $In_xGa_{1-x}As$ layers, introduced by the lattice relaxation, can cause the increase in the leakage current, attributable to TAT, resulting in degradation of gate controllability and S.S. in the $In_xGa_{1-x}As$ QW tunnel FETs. Therefore, the control of the defects and dislocations generated in high-In-content $In_xGa_{1-x}As$ QW layers is one of the most important issues for enhancing the performance of InxGa1-xAs QW tunnel FETs.

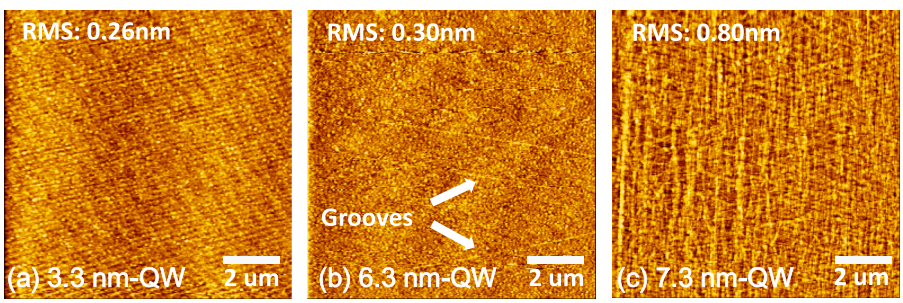

FIG. 20. AFM images of InAs QW surfaces: (a) 3.3-nm-thick InAs QW, (b) 6.3-nm-thick InAs QW, and (c) 7.3-nm-thick InAs QW.

VII. CONCLUSION

We have proposed the planar-type $In_xGa_{1-x}As$ QW tunnel FETs with Zn-diffused sources for achieving high I_{on} without an increase in I_{off}. The design of the QW thickness and the In content of the $In_xGa_{1-x}As$ QW structures for tunnel FET applications has been presented in terms of the effective bandgap of the QW layers. We fabricated the planar-type $In_xGa_{1-x}As$ QW tunnel FETs by using the $In_xGa_{1-x}As$ QW structures grown by MOVPE and confirmed the device operation. It has been found that the thinner QW thickness results in steeper S.S., while the higher In content and the thicker QW thickness lead to higher I_{on}. These tendencies are consistent with the calculation results of E_{geff}. The $S.S._{min}$ of 62 mV/dec at $V_D = 150$ mV was achieved for the 3.2-nm-thick $In_{0.67}Ga_{0.33}As$ QW tunnel FET. Also, the highest I_{on} of 11 $\mu A/\mu m$ at $V_D = 1$ V and $V_G = 1$ V and the I_{on}/I_{off} ratio higher than 10^4 were obtained for the 6.3-nm-thick InAs QW tunnel FET. It was also observed that the leakage current of InAs QW tunnel FETs increases drastically for the InAs QW thicker than 5 nm in thickness, which is attributable to lattice relaxation. Thus, it is important to minimize the densities of defects and dislocations in high-In-content $In_xGa_{1-x}As$ layers for maintaining the low leakage current, resulting in the superior performance of $In_xGa_{1-x}As$ QW tunnel FETs.

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