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Phosphorus-doped polycrystalline silicon passivating contacts via spin-on doping

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ABSTRACT

Polycrystalline silicon (poly-Si) passivating contacts are promising technologies to promote the efficiency of silicon solar cells, due to their low carrier recombination and low contact resistivity. In this work, we present phosphorus spin-on doping as an alternative doping method to fabricate high performance poly-Si passivating contacts. The influences of thermal treatments and intrinsic amorphous Si thickness on poly-Si passivating contact quality were investigated. A high implied open-circuit voltage of above 730 mV together with a low contact resistivity below 4 mΩ·cm^2 were obtained for 100 – 230 nm thick poly-Si layers after a thermal treatment at 975 °C for 60 min followed by a forming gas annealing. The promising results presented in this work imply that phosphorus spin-on doping can be an effective doping method alternative to conventional $POCl_3$ diffusion.

1. Introduction

After years of development, the passivating contact has become an essential way for crystalline silicon (c-Si) solar cells to approach the theoretical maximal conversion efficiency of 29.4% [1]. An ideal passivating contact should provide high carrier selectivity with low carrier recombination and low contact resistivity at the same time [2]. Among diverse passivating contacts, polycrystalline silicon (poly-Si) passivating contacts have been proven to be a promising approach for high-efficiency solar cells, due to excellent carrier selectivity [2–9]. The advantages of poly-Si passivating contacts come from the composition of an ultrathin (thickness 1 – 2.5 nm) silicon oxide (SiO_x) layer capped by a layer of heavily doped poly-Si [2]. The ultrathin SiO_x interlayer will not only passivate the surface of the c-Si substrate, but also impede dopant diffusion from the poly-Si into the c-Si during the dopant activation process [10–12].

Poly-Si passivating contacts can be doped via *in-situ* doping and *ex-situ* doping methods. For *in-situ* methods, dopants (phosphorus or boron are commonly used) are introduced during plasma enhanced chemical vapour deposition (PECVD) [13–19] or low pressure chemical vapour deposition (LPCVD) [20–22]. The *ex-situ* doping sources can be gas dopants [10,23–26], ion dopants [27–32], liquid dopants [33–35], and others. The liquid doping methods mainly contain screen-printing, inkjet-printing, and spin-on doping. This kind of method has several advantages: (i) they involve less dangerous materials; (ii) the liquid dopant inks can contain a wide variety of chemical elements (dopant species) with different concentrations; and (iii) the doped regions can be patterned easily [36,37]. Liquid dopants have been successfully implemented into Si solar cell fabrication previously. Phosphorus dopant was screen-printed directly on Czochralski (Cz) p-type wafers to form a selective emitter [38], which yielded an effective lifetime of 350 μs and an open-circuit voltage of 625 mV, leading to 18% cell efficiency. Recently, research on inkjet-printed P dopant for poly-Si contacts has been carried out by Kiaee *et al.*, demonstrating an implied open-circuit voltage (iV_{OC}) value of 733 mV [39].

Another promising method using liquid dopants is the spin-on

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doping (SOD), which is able to spread liquid dopants uniformly on a silicon substrate [40–42]. The dopants are used to form ultra-shallow junctions in micro-electronic device fabrication using a single thermal treatment [43,44]. For silicon solar cell fabrication, spin-on doping processes are also applied to form n-type or p-type doped silicon regions [45–47]. Hamammu *et al.* used a phosphorus-containing spin-on glass "Filmtronics P509" as a P dopant source to realize a solar cell of 17.1% efficiency [45]. Furthermore, Martínez *et al.* reported that the emitter region of a solar cell fabricated using a spin-on dopant source (also Filmtronics P509) exhibited comparable cell performance to an emitter formed by gas dopant (PH_3) diffusion [46]. Meanwhile, Singha *et al.* optimized the diffusion of boron spin-on dopant to form p-type emitters with low sheet resistance (< 60 Ω/square) and high iV_{OC} without any surface passivation process (575 – 600 mV) [48], leading to a simulated cell efficiency of 14.8%. These promising results for silicon solar cells motivate the utilization of spin-on doping to fabricate poly-Si passivating contacts. Fogel *et al.* deposited intrinsic silicon (i-Si) layers bifacially above SiO_x/c-Si/SiO_x using PECVD or LPCVD [49], and then applied the phosphorus or boron spin-on glasses onto the symmetric i-Si/SiO_x/c-Si/SiO_x/i-Si structures, followed by high temperature annealing to drive-in and activate dopants. After a hydrogenation process, the samples with doped PECVD and LPCVD poly-Si showed the final iV_{OC} of 708 mV and 727 mV respectively for P doping, and 667 mV and 689 mV respectively for B doping. Additionally, Young *et al.* fabricated Ga-doped poly-Si passivating contacts by using gallium spin-on dopants, showing an iV_{OC} value more than 730 mV [50].

The above results show that excellent poly-Si passivating contacts can be realized via spin-on doping. However more efforts are required to make this technique more reliable for poly-Si passivating contacts fabrication in industry. In this work, we implemented wafers prepared using industrial processes and studied the influences of the drive-in process (temperature and dwell time) and intrinsic amorphous silicon thickness on the properties of phosphorus-doped poly-Si passivating contacts. The results may help other researchers to adjust the spin-on doping process and acquire aimed performance.

2. Experimental details

Symmetrical samples were prepared on 2 in. × 2 in. square (100)-oriented industrially planarized n-type Cz silicon wafers. The thickness and resistivity were 160 – 170 μm and 5.5 ± 0.4 Ω·cm, respectively. Such high resistivity wafers were chosen to minimize the impact of bulk recombination on the effective lifetime and to enable accurate characterisation of the quality of the surface passivation. After a wafer cleaning process, the ultrathin silicon oxide (SiO_x) layers (thickness < 2 nm [10,23,51]) were formed by thermal oxidation at 600 °C for 5 min in pure oxygen ambient at a flow of 2 standard litres per minute. The intrinsic amorphous Si (a-Si) layers were prepared in an industrial low-pressure chemical vapour deposition (LPCVD) tool at 520 – 550 °C [31,52,53] with three different thicknesses (100, 175 and 230 nm). The sample preparation up to here was performed at Jinko Solar using industrial mass production tools. The thicknesses of the intrinsic a-Si layers were determined at this stage of the sample preparation using a focused ellipsometer (J.A. Woollam ESM-300). The symmetric a-Si/SiO_x/c-Si/-SiO_x/a-Si substrates were cleaned by RCA solutions. Thickness of a-Si consumed during RCA is likely to be negligible, compared to the thickness of the whole a-Si layer. Both sides of these substrates were then coated by phosphorous-containing spin-on glass solution (P-250, [P] 5 × 10^{21} cm^{-3}, Desert Silicon) using a spin coater (Laurell WS-650-23NPPB). The spin-on glass (SOG) films were formed after a series of drying processes, including venting (room temperature for 10 min in air), soft baking (90 °C for 10 min in air) and hard baking (200 °C for 5 min in air). The gradual increase in drying temperature is beneficial for avoiding cracks in the SOG films. Higher spin speed or spin speed acceleration was found to form thinner SOG films. The average thickness of SOG films for the optimized spin coat parameters used in this experiment is ~260 nm after the drying processes. Afterwards, the as-coated samples were thermally treated in an N_2 atmosphere using a quartz tube furnace to drive-in and activate the dopants at various temperatures and dwell times. The drive-in temperature was varied from 900 °C to 1050 °C for 60 min and the annealing dwell time was varied from 30 min to 120 min at 975 °C. After high temperature treatments, the deposited silicon will become polycrystalline phase (poly-Si). Subsequently, the phosphorus-silica glasses were removed in 3% HF solution for 3 min. Finally, the samples were hydrogenated using forming gas annealing (FGA, 5% H_2, 95% Ar) at 400 °C for 30 min.

The corresponding implied open circuit voltage (iV_{OC}) values were measured using the Photoconductance Decay (PCD) method with a Sinton WCT-120 lifetime tester [54] before and after the FGA process. The surface saturation current density, J_0, of the samples were extracted from the PCD measurements using the Kane-Swanson method [55]. The active dopant profiles were measured by electrochemical capacitance-voltage (ECV) measurement (WEP Wafer Profiler CVP21). The contribution of Auger recombination to the overall J_0 is simulated using EDNA2 [56], with the measured active dopant profile as input. The contact resistivity was obtained using the Cox-Strack method [57], with 250 nm thick Al circular pads of various diameters evaporated on one side of the sample, and 250 nm thick Al fully covering the other side. The resolution of the contact resistivity determination is influenced by the wafer thickness, the wafer resistivity and the size of Al circular pad. Here, due to the uncertainty caused by varying silicon substrate resistivities, a detection limit of contact resistivity was estimated. equations (1)–(3) were introduced from Ref. [57]. R_T represents the measured total resistance as the sum of the spreading resistance (R_S), the contact resistance (R), and the residual resistance (R_0). Using equation (2), R_S can be calculated from the metal pad diameter (d), the c-Si substrate resistivity (ρ), and the c-Si substrate thickness (t). The second term, contact resistance R, is based on d and the specific contact resistance (R_C), which covers the carrier transport through the whole stack of Al/doped poly-Si/SiO_x. The last term, R_0, is independent of d and covers residual resistance due to the substrate or the contact resistance of the full area back side contact. To attain the contact resistivity detection limit, we firstly found the largest absolute deviation of measured ρ from the mean ρ (5.5 Ω·cm), and worked out the ratio of this deviation over the mean ρ. Then this ratio was multiplied by R_T to show the largest absolute deviation of R_T, which acted as the upper limit of R when R values were too low to be measured accurately. Afterwards the R upper limit was used together with equation (3) to calculate the upper limit of R_C, *i.e.* contact resistivity detection limit. As the result the detection limit of contact resistivity was found to be ~4.0 mΩ·cm^2 in this work.

$$R_T = R_S + R + R_0 \tag{1}$$

$$R_S = \left(\frac{\rho}{d\pi}\right)\arctan\left(\frac{4t}{d}\right) \tag{2}$$

$$R = \frac{4R_C}{\pi d^2} \tag{3}$$

3. Results and discussion

Here we present a study on the performance of poly-Si passivating contacts by closely examining three key process parameters: drive-in temperature, drive-in dwell time, and thickness of the poly-Si layer. The electronic performances of the poly-Si passivating contacts are evaluated by using their implied open-circuit voltages (iV_{OC}) and contact resistivity values (ρ_c).

3.1. Impact of drive-in temperature

Fig. 1a shows the impact of the drive-in temperature on the passivation quality, via the iV_{OC}, of poly-Si passivating contacts before (full

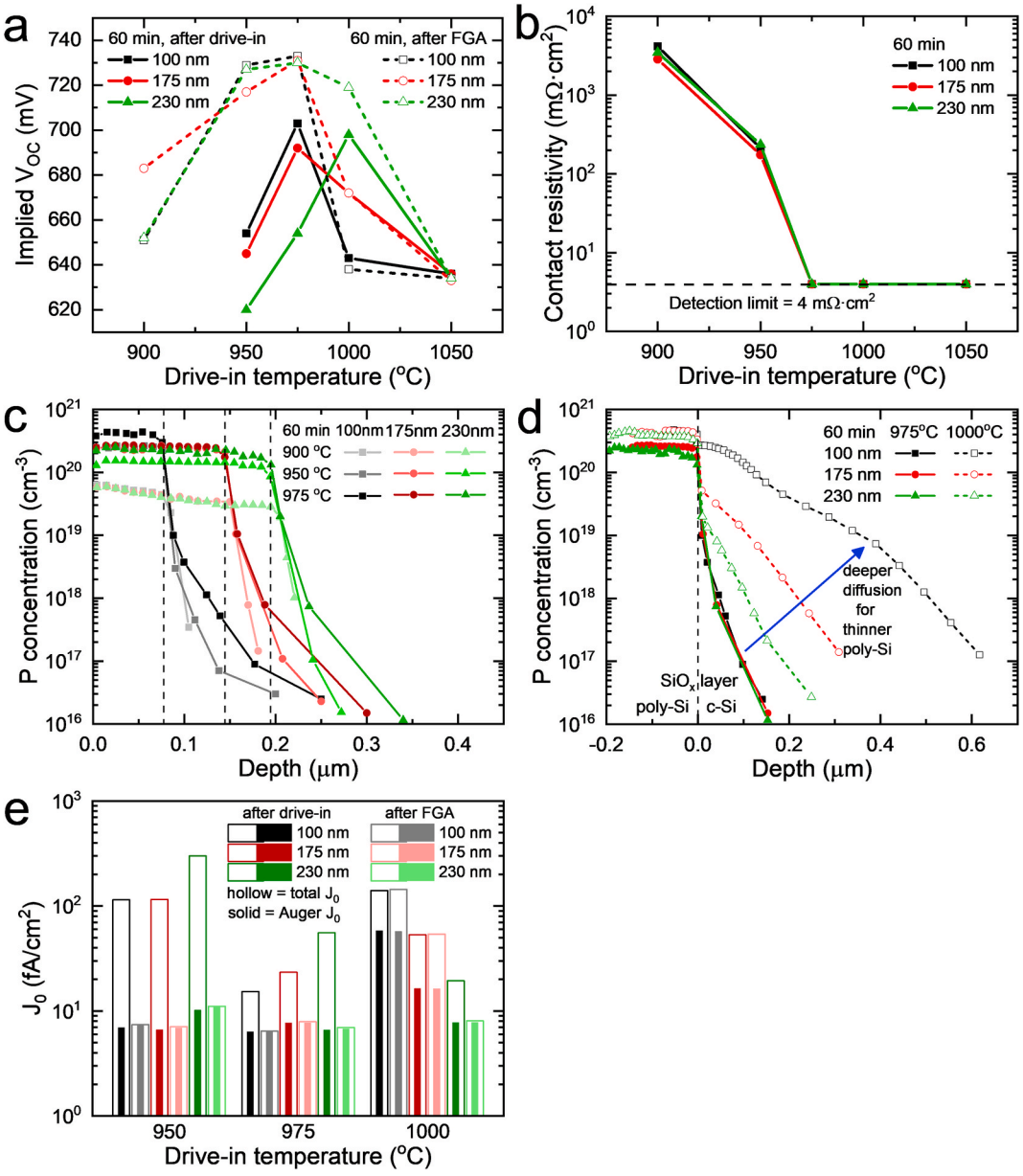

Fig. 1. (a) iV_{OC} values of P-doped samples for poly-Si thicknesses of 100 nm (black), 175 nm (red) and 230 nm (green) annealed for 60 min at different temperatures (filled symbols, solid lines) and after FGA (open symbols, dashed lines); (b) the corresponding values of contact resistivity after FGA; the corresponding doping profiles of 100 nm, 175 nm and 230 nm poly-Si samples annealed at (c) 900 – 975 °C and (d) 975 – 1000 °C. The dashed lines indicate the position of the SiO_x interlayers. (e) Measured total surface J_0 (hollow bars) and simulated contribution of Auger recombination (solid bars) for the three poly-Si thicknesses before and after FGA. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

symbol, solid line) and after FGA (open symbol, dashed line). The drive-in time was set to 60 min and three different poly-Si thicknesses (100 nm in black, 175 nm in red and 230 nm in green) were used. Before the forming gas annealing, the iV_{OC} values for all poly-Si thicknesses first increase and then decrease as the drive-in temperature increases. The iV_{OC} data for 900 °C is too low to be obtained under the same measurement conditions as for other samples. While the iV_{OC} values for 100 and 175 nm poly-Si reach the highest values of 703 and 692 mV respectively at 975 °C, the 230 nm poly-Si sample has the highest iV_{OC} of 698 mV at 1000 °C. Similar iV_{OC} trends are observed for the samples after FGA. As the drive-in temperature increases, the iV_{OC} values of the three poly-Si thicknesses all increase, reaching their maximum above 730 mV at 975 °C. When the temperature increases further, the iV_{OC} values all decrease remarkably with an even greater reduction for the thinner poly-Si layer. The highest iV_{OC} value of 733 mV was obtained for 100 nm poly-Si driven-in at 975 °C.

The trend above mentioned agrees well with results obtained by Feldmann *et al.* and Stodolny *et al.*, who ascribed this trend to the band bending [11] and field-effect [58]. By closely examining the doping profiles, as shown in Fig. 1c, we speculate similar passivation mechanisms can explain the results presented in this work. A high doping level in the poly-Si and a considerable dopant diffusion into the c-Si are essential to achieve good passivation. For drive-in temperatures below the optimal point, a higher temperature induces a higher doping level in the poly-Si, which is more obvious for thinner poly-Si layers. The high concentration of activated dopants in poly-Si may form a strong band bending in c-Si below SiO_x interlayer, which results in a high built-in voltage [11]. Meanwhile, a higher temperature leads to higher active dopant concentration near SiO_x/c-Si interface and deeper dopant diffusion into the c-Si substrate, which presumably contribute to

field-effect passivation [59]. The field-effect helps to suppress the minority carrier density near the SiO_x/c-Si interface and reduce interface carrier recombination. The simulated recombination mechanisms shown in Fig. 1e reveals that for the three poly-Si thicknesses, the temperature increase from 950 °C to 975 °C results in almost unchanged Auger recombination but reduced total recombination. This trend could be due to stronger band bending and field-effect, which is especially obvious for thinner poly-Si.

However, when the drive-in temperature is higher than the optimal point, the iV_{OC} values for all three poly-Si thicknesses decrease sharply to ~635 mV at 1050 °C. The decrease in passivation quality at excessively high temperatures has also been reported for $POCl_3$ diffused [10,60,61] and P ion implanted [30,62,63] poly-Si contacts, even though in these cases the optimal drive-in temperatures are substantially lower (800 – 900 °C). This divergence is probably the consequence of the robust dopant-rich glass/poly-Si interface [58,59,61], but also the crystallized thick intrinsic silicon layer [10,30,60,62,64] and the difference in SiO_x interlayer thickness may have an impact. Fig. 1d compares the doping profiles of samples at 975 °C and 1000 °C. For the sample with 230 nm poly-Si at 1000 °C, the doping level in the poly-Si becomes higher, but dopant diffusion into the c-Si remains relatively shallow. These factors likely lead to lower total J_0 as shown in Fig. 1e and increase in iV_{OC}. However, for 100 and 175 nm poly-Si at 1000 °C, the dopant diffusion into the c-Si is relatively deep. The result implies that some degree of break-up in the SiO_x interlayer occurs [65], and considerable densities of defects are formed near the SiO_x/c-Si interface. The remarkable increase of total J_0 as well as Auger J_0 displayed in Fig. 1e supports that the heavier interface recombination and increased Auger recombination both contribute to poorer passivation [10,64].

Moreover, the passivation improvement induced by FGA varies with

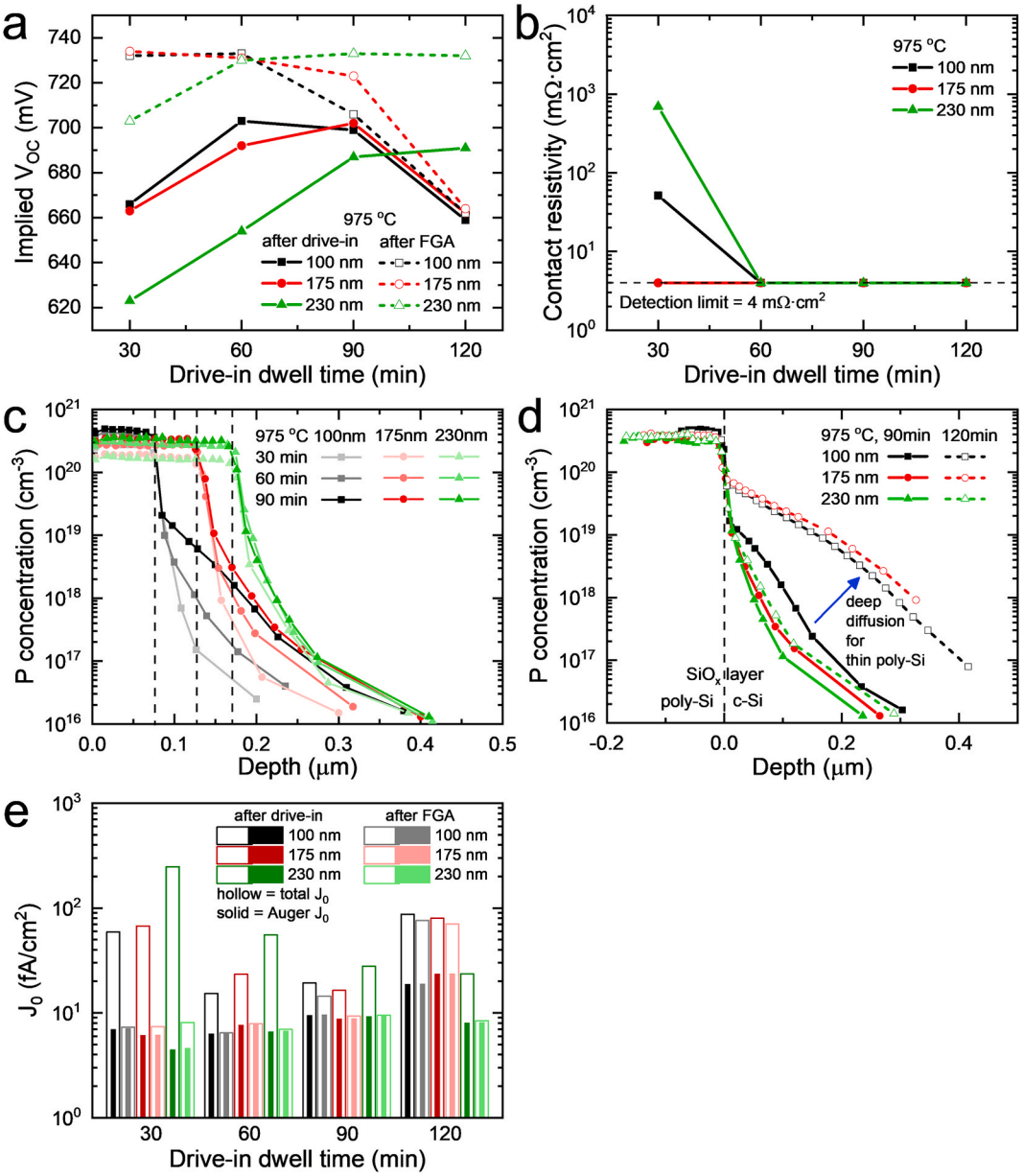

Fig. 2. (a) iV_{OC} values of P-doped samples for poly-Si thicknesses of 100 nm (black), 175 nm (red) and 230 nm (green) annealed at 975 °C for different drive-in durations (filled symbols, solid lines) and after FGA (open symbols, dashed lines); (b) the corresponding values of contact resistivity after FGA; the corresponding doping profiles of 100 nm, 175 nm and 230 nm poly-Si samples annealed at 975 °C for (c) 30 – 90 min and (d) 90 – 120 min. The dashed lines indicate the position of the SiO_x interlayer. (e) Measured total surface J_0 (hollow bars) and simulated contribution of Auger recombination (solid bars) for the three poly-Si thicknesses before and after FGA. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

drive-in temperature. For the temperature below the optimal, FGA endows significant iV_{OC} increases for all three poly-Si thicknesses; while for excessively high temperatures, FGA plays a minor role or even has no impact on improving the passivation quality. For example, for 175 nm poly-Si, the iV_{OC} improvement for 950 °C drive-in is ~72 mV, but the improvement for 1000 °C drive-in is almost negligible. Comparing doping profiles for 175 nm poly-Si at 950 °C and 1000 °C (in Fig. 1c and d respectively), we find a higher dopant concentration and deeper dopant diffusion in the c-Si at 1000 °C. This may imply more defects at the SiO_x/c-Si interface upon driving-in at 1000 °C [30]. Combining the EDNA2 results in Fig. 1e we could deduce that, after 950 °C drive-in the SiO_x break-up is slight and the defects in doped poly-Si and near SiO_x interlayer can be passivated effectively. But after 1000 °C drive-in, the SiO_x interlayer for thin poly-Si is damaged heavily and Auger recombination is also increased significantly, which reduces the impact of FGA.

Fig. 1b presents the corresponding contact resistivity of samples shown in Fig. 1a. When the drive-in temperature increases from 900 °C to 975 °C, the contact resistivities of all samples decrease substantially from over 3×10^3 mΩ·cm^2 to below the detection limit of ~4 mΩ·cm^2. With further higher drive-in temperature, the contact resistivities remain below the detection limit. The pronounced reduction and low values of contact resistivity can be explained by the increased dopant concentration in the poly-Si and in the c-Si near the SiO_x/c-Si interface, and more break-up of the oxide interlayer produced by higher drive-in temperatures [65].

3.2. The impact of drive-in dwell time

After exploring drive-in temperature, the impact of drive-in duration was studied at a temperature of 975 °C. Fig. 2a displays the iV_{OC} values for 100 nm (black), 175 nm (red) and 230 nm (green) poly-Si as a function of drive-in dwell time before (filled symbols, solid lines) and after FGA (open symbols, dashed lines). After the drive-in process, samples show similar iV_{OC} trends as those for various drive-in temperatures described above. The iV_{OC} values for all poly-Si thicknesses increase for longer drive-in dwell time, reaching optimal points, and then turn to decrease for further prolonged drive-in dwell time. The highest iV_{OC} for 100 and 175 nm poly-Si are 703 and 702 mV for 60 min and 90 min drive-in respectively. For the case of 230 nm poly-Si, the iV_{OC} increases with longer drive-in time and saturates at a value of 691 mV at 120 min. After FGA, the passivation quality displays different dependences on drive-in dwell time for various poly-Si thicknesses. For thin poly-Si (*i.e.*, 100 and 175 nm), iV_{OC} has a decreasing trend with longer drive-in dwell time, whereas thick poly-Si (230 nm) sample exhibits an increasing trend. High iV_{OC} values above 730 mV are observed for all three poly-Si thicknesses for 60 min drive-in process.

Fig. 2c and d presents the doping profiles for the three poly-Si thicknesses for varied drive-in dwell time. It can be seen that with longer drive-in dwell time, the doping levels in poly-Si increase and at the same time the dopant in-diffusions into c-Si become deeper, which is similar to the case with high drive-in temperature, as shown in Fig. 1d. Similar trends in doping profiles may suggest that the behaviors here could be explained by similar mechanisms as discussed in the previous section. Under the conditions of little interfacial oxide break-up (or no oxide break-up), a high doping concentration in the poly-Si implies a large difference in doping level between poly-Si and c-Si, leading to a substantial band bending and a high built-in voltage in c-Si below the SiO_x interlayer [11]. At the same time, a deeper dopant in-diffusion presumably forms a stronger field-effect [59], which shields minority carriers from reaching the SiO_x/c-Si interface, thus reducing carrier recombination. Fig. 2e demonstrates the measured total recombination and the simulated Auger recombination for the three poly-Si thicknesses for 30 – 120 min drive-in. The total surface J_0 values decrease with longer drive-in dwell time until reaching a minimum after 90 min, while the fractions of Auger recombination become larger. This may indicate a balance between decreased total J_0 and increased Auger J_0 during the prolonged drive-in process. Therefore, the dominating strong band bending together with field-effect over considerable Auger recombination may result in an increasing iV_{OC} for longer drive-in dwell time until their optimums are reached. As mentioned in the previous section, a thicker poly-Si layer slows down the diffusion and therefore a longer drive-in dwell time is required to obtain optimum iV_{OC} [58,66].

Similar to the case of excessive drive-in temperature, the iV_{OC} values for 100 and 175 nm poly-Si both exhibit decreasing trends for excessively long drive-in dwell time, down to ~660 mV for 120 min. Fig. 2d shows that the dopant in-diffusions for 100 and 175 nm poly-Si increased strongly from 90 min to 120 min drive-in, while the dopant in-diffusion for 230 nm poly-Si only increased slightly. These doping profiles in c-Si could be responsible for the J_0 variation presented in Fig. 2e, in which both the total J_0 and Auger J_0 are notably higher for 100 and 175 nm poly-Si after 120 min drive-in than the case for 90 min drive-in. Therefore, the low iV_{OC} values after excessive drive-in may be the consequence of heavy carrier recombination, which results from numerous dopants diffused into c-Si [67], and from a large fraction of SiO_x interlayer break-up [10,64].

In terms of iV_{OC} difference induced by FGA, less drive-in dwell time leads to larger improvement in iV_{OC} value. This trend can be observed for all three poly-Si thicknesses. For example, for 175 nm poly-Si 30 min drive-in is related to iV_{OC} improvement of 70 mV from FGA, but almost no improvement is obtained for 120 min drive-in. Fig. 2e exhibits that for the 100 nm thick poly-Si and drive-in dwell time up to 60 min, the total J_0 can be reduced by FGA, which means the major defects can be hydrogenated by FGA. However, for drive-in dwell time more than 60 min, the decrease in total J_0 after FGA is limited, suggesting that the major defects may be SiO_x interlayer distortion and Auger recombination centers. Therefore, as shown by the doping profiles in Fig. 2c and d, a longer drive-in process drives more dopants through SiO_x interlayer into c-Si, forming more damage on the SiO_x interlayer and higher Auger recombination, thus leading to less iV_{OC} improvement by FGA.

Fig. 2b presents the corresponding contact resistivity of samples shown in Fig. 2a after drive-in at 975 °C for various dwell times. The values of contact resistivity of 100 and 230 nm poly-Si samples decrease from ~50 and ~700 mΩ·cm^2 after 30 min drive-in to below the detection limit of ~4.0 mΩ·cm^2 after 60 min drive-in, respectively. The contact resistivity of 175 nm poly-Si sample is below the detection limit for all tested dwell times. With longer drive-in, more dopants are diffused into poly-Si and c-Si substrate, which could decrease the resistivity towards majority carriers. Besides, the strong dopant in-diffusion for 100 and 175 nm poly-Si indicates that considerable break-up appears in SiO_x interlayer, which is beneficial to carrier transportation [65].

4. Conclusions

In summary, we explored the ability of phosphorus spin-on doping as an effective doping method for n-type poly-Si passivating contacts. The effect of drive-in temperature, drive-in dwell time as well as intrinsic a-Si thickness on the passivating contact quality was studied. For the intrinsic Si thickness of 100 – 230 nm, the iV_{OC} values after FGA increase with higher drive-in temperature and then decrease for excessively high temperature, presenting an optimum at 975 °C. Moreover, the drive-in dwell time required for optimum iV_{OC} after FGA shows an increase with intrinsic Si thickness (i.e. 60 min for 100 and 175 nm, and 90 min for 230 nm). From the ECV profiles of both drive-in temperature and dwell time cases, we found that the passivation quality depends strongly on the amount of dopants in the poly-Si layer and the c-Si near the SiO_x interlayer. After the optimization process shown in this work, phosphorus doped poly-Si passivating contacts fabricated by spin-on doping achieved an implied V_{OC} above 730 mV together with a contact resistivity below 4 mΩ·cm^2, which are comparable with the performance realized by traditional $POCl_3$ diffusion.

CRediT authorship contribution statement

Zetao Ding: Conceptualization, Methodology, Investigation, Visualization, Writing - original draft. **Di Yan:** Conceptualization, Methodology, Investigation, Visualization, Writing - review & editing, Supervision. **Josua Stuckelberger:** Methodology, Investigation, Visualization, Writing - review & editing, Supervision. **Sieu Pheng Phang:** Methodology, Visualization, Writing - review & editing. **Wenhao Chen:** Investigation. **Christian Samundsett:** Investigation. **Jie Yang:** Investigation, Resources. **Zhao Wang:** Investigation, Resources. **Peiting Zheng:** Investigation, Resources. **Xinyu Zhang:** Investigation, Resources, Supervision, Project administration. **Yimao Wan:** Conceptualization, Writing - review & editing, Supervision, Project administration. **Daniel Macdonald:** Writing - review & editing, Supervision, Project administration.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Appendix A. Supplementary data

Supplementary data related to this article can be found at https://doi.org/10.1016/j.solmat.2020.110902.

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